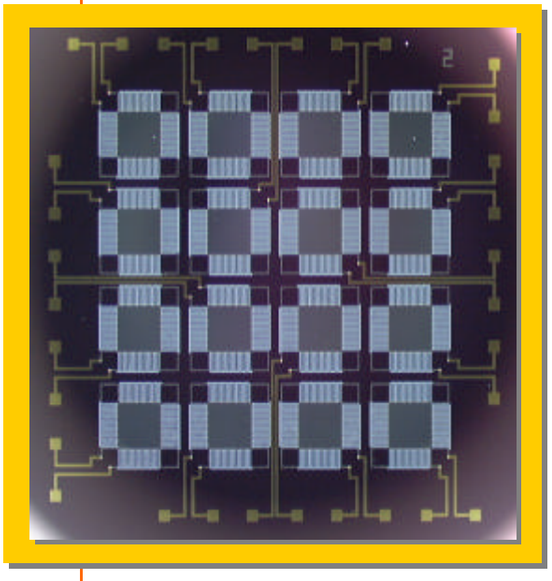
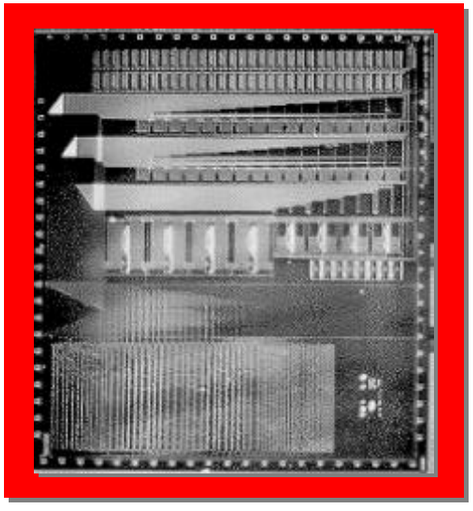
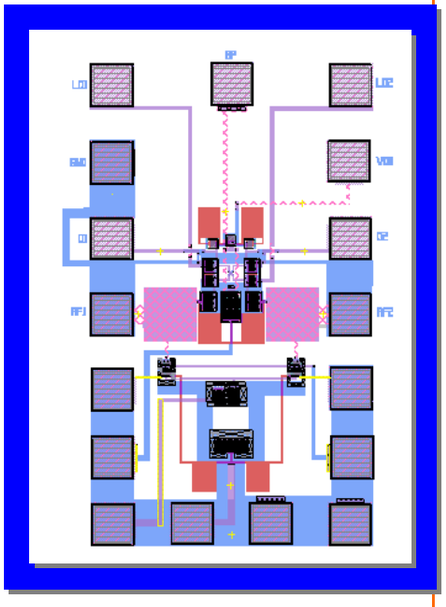
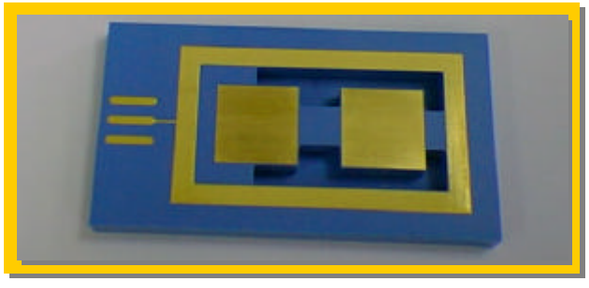
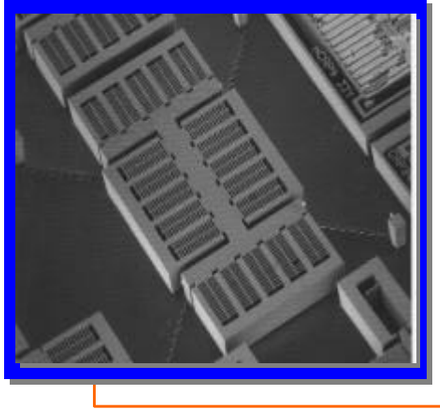
Technology Progress 7/99 - 12/99

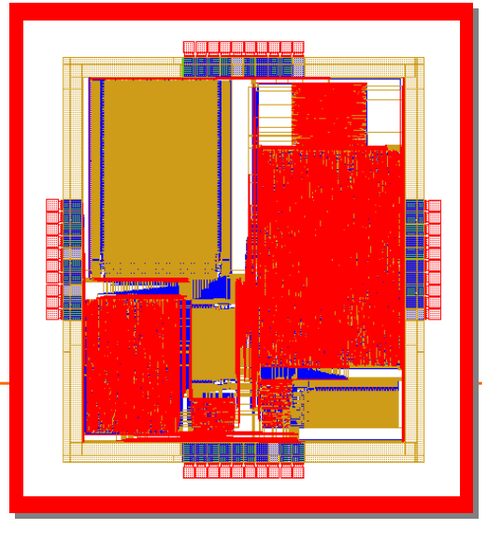


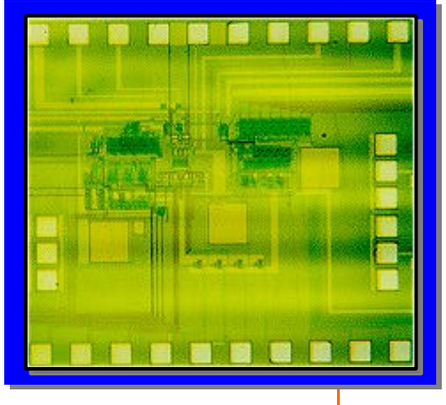












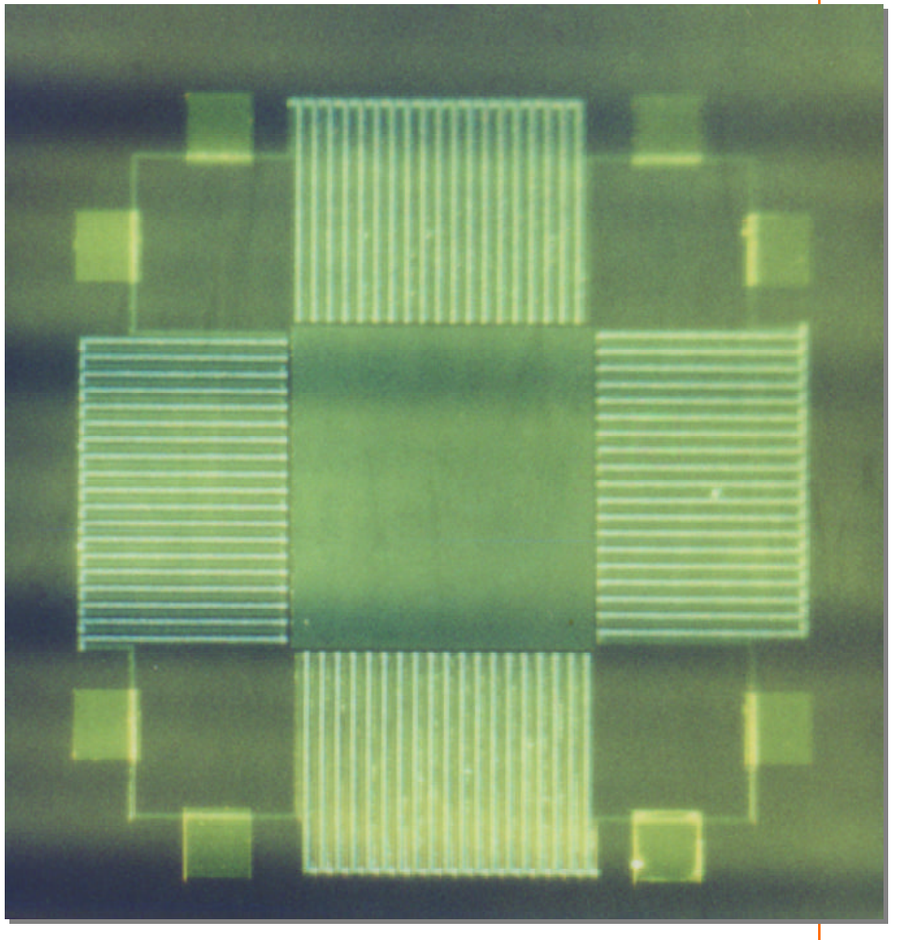
LWIM in the Field

Continuous system demonstrations and research guidance

• Sept 96	29 Palms	USMC data collection
• Sept 96	29 Palms	USMC Desert Fire
• Dec 96	29 Palms	USMC Steel Knight
• April 97	29 Palms	USMC Desert Scimitar
• June 97	Aberdeen Proving Ground	Army
• October 97	USS Rushmore	US Navy
• December 97	29 Palms	Steel Knight
• February 97	Army NTC	US Army data acquisition
• April 98	Army NTC	US Army data acquisition
• September 99	Aberdeen PG	US Army data acquisition

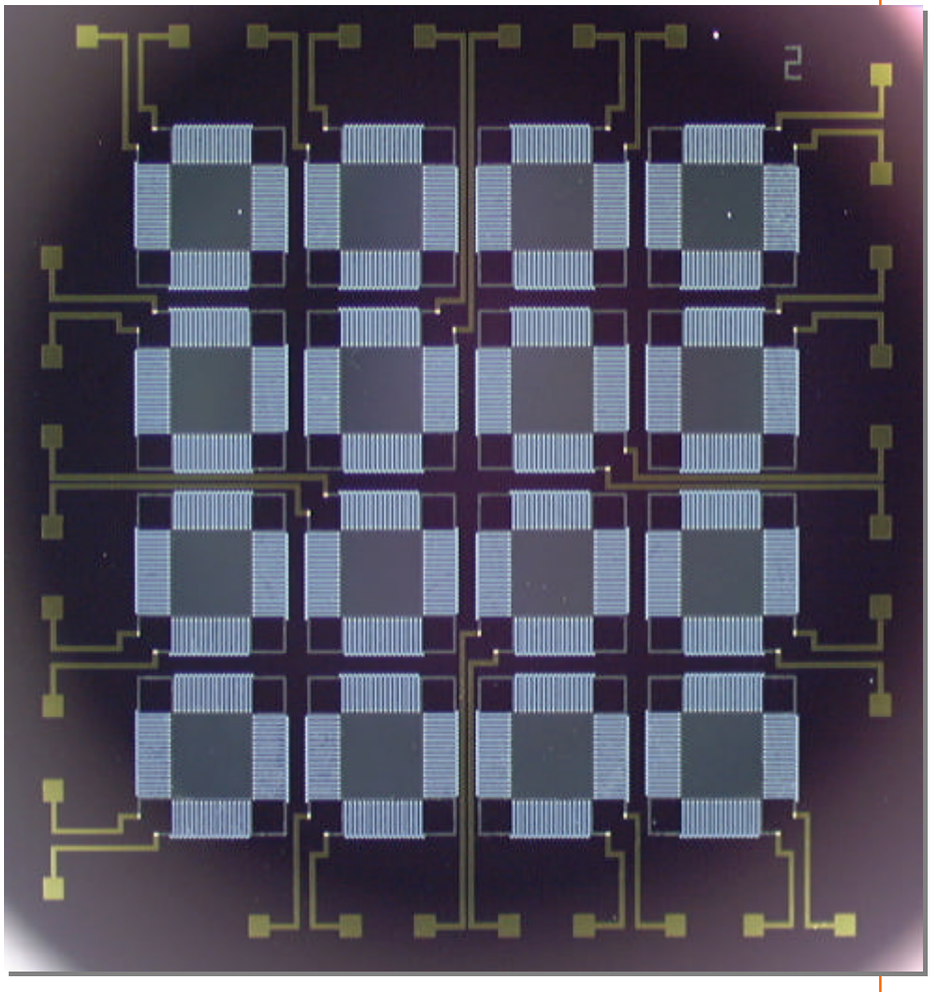
Micropower Infrared Sensor Element

- Bi-Sb junctions -- 105μV/K per junction
- 0.5 μm Silicon Nitride thermal isolation membrane
- Low resistance metallic thermopiles yield low thermal noise
- Electrical resistance is about 60 kΩ for a 116 junction thermopile



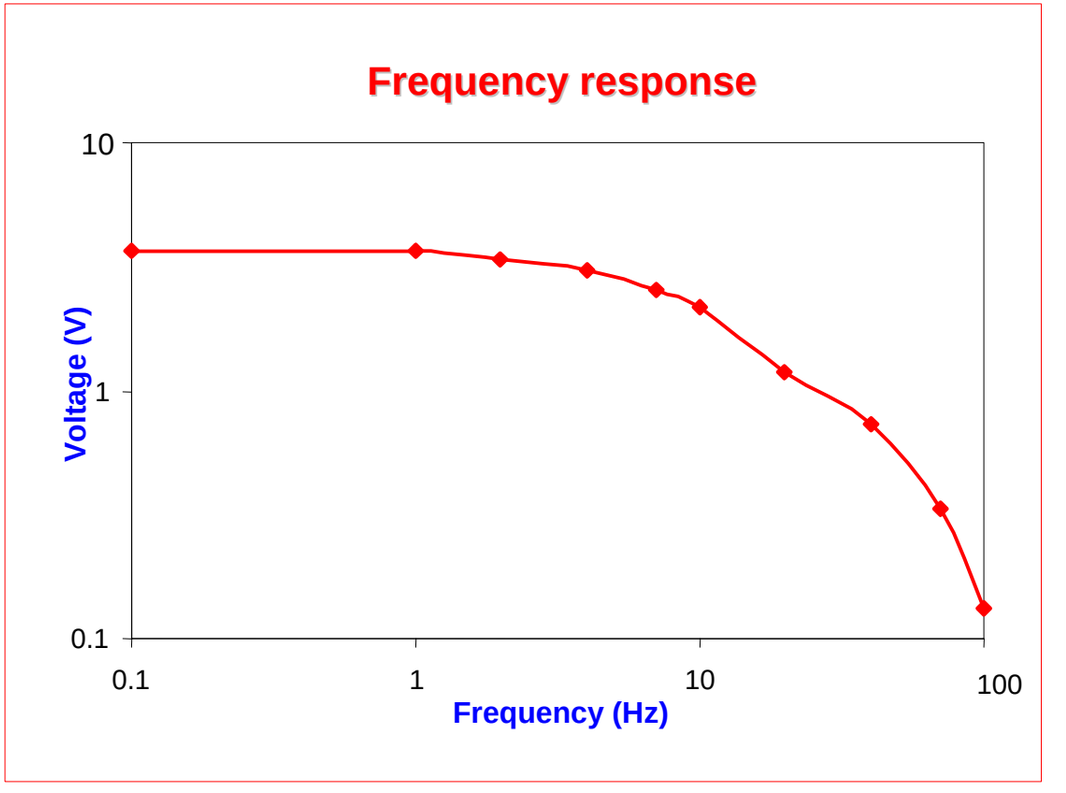
4 ´4 Sensor Array

- A 4x4 array of infrared sensors allows diverse motion detection capability
- Significant extension over conventional single and dual element devices

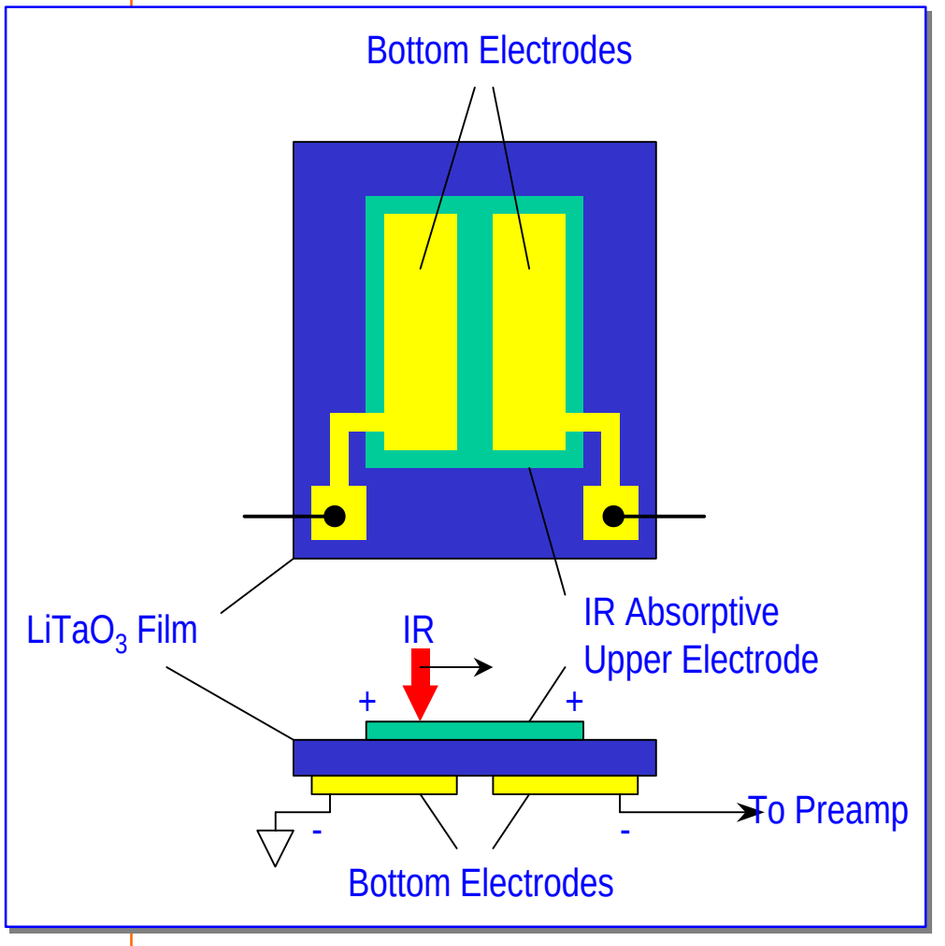


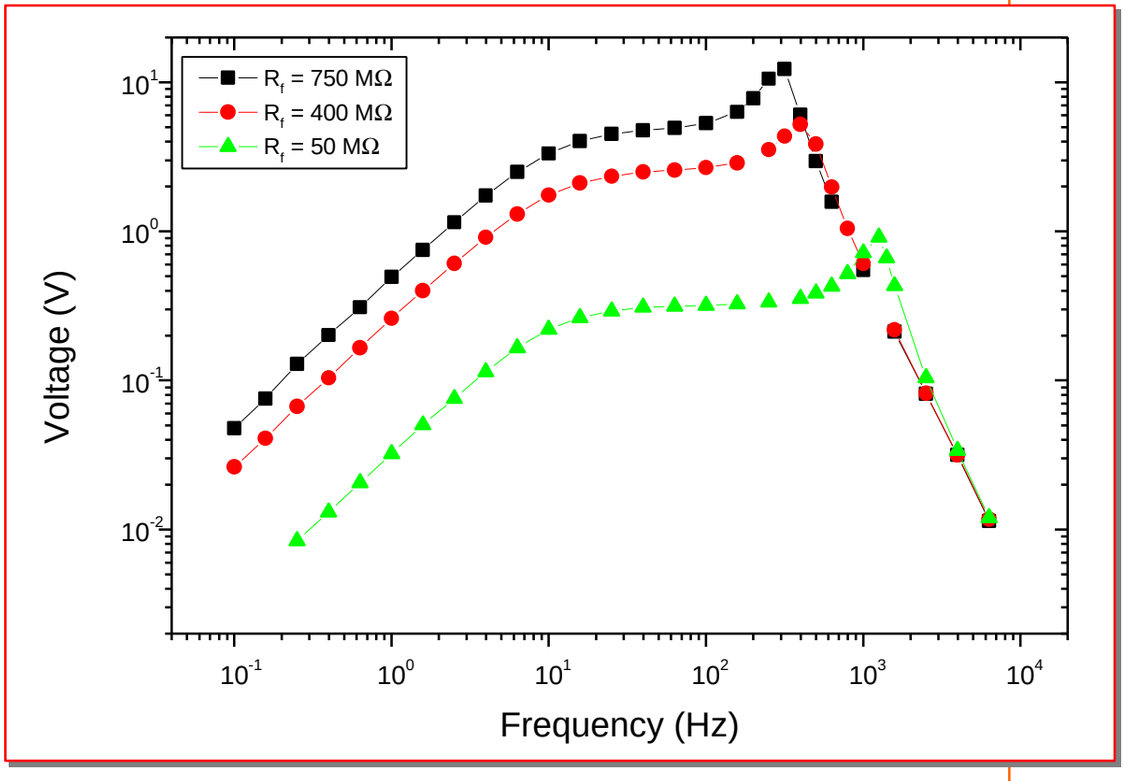
Thermopile Performance Characteristics

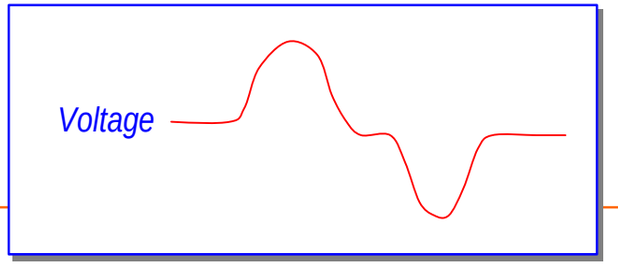
- Responsivity of 2.1 V/W with no gain
- Estimated NEP of 1.7×10^{-8} (W/√Hz)
- Transient response starts dropping off at a few Hz



Pyroelectric Infrared Sensor



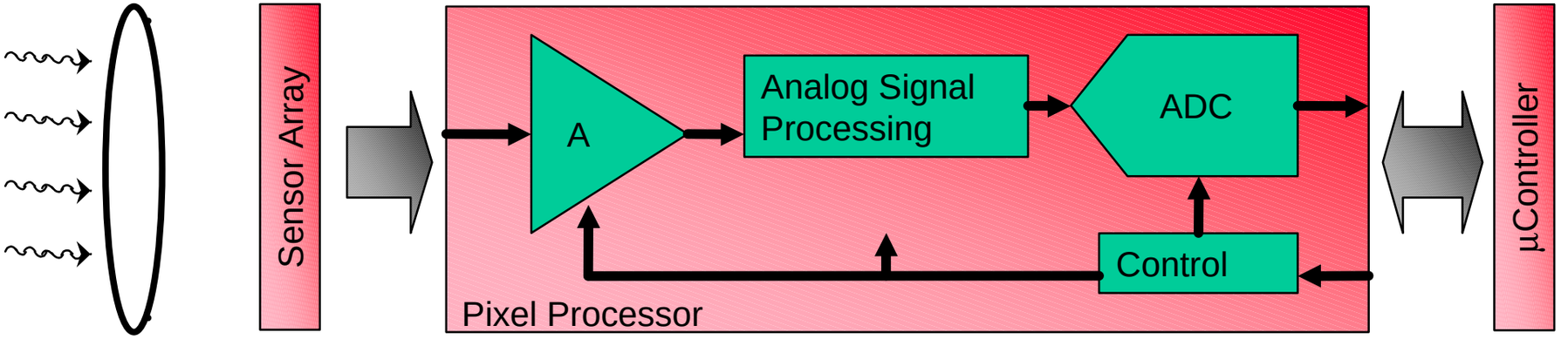




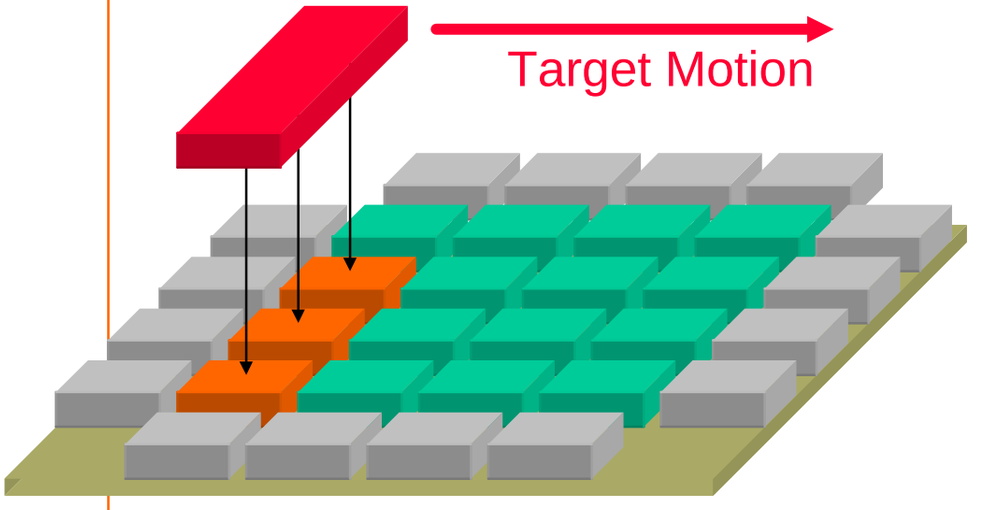
Infrared Focal Plane System

- The infrared focal plane system is composed of several elements:
  - micromachined thermal infrared sensor die
  - multifunction pixel processor
  - microcontroller

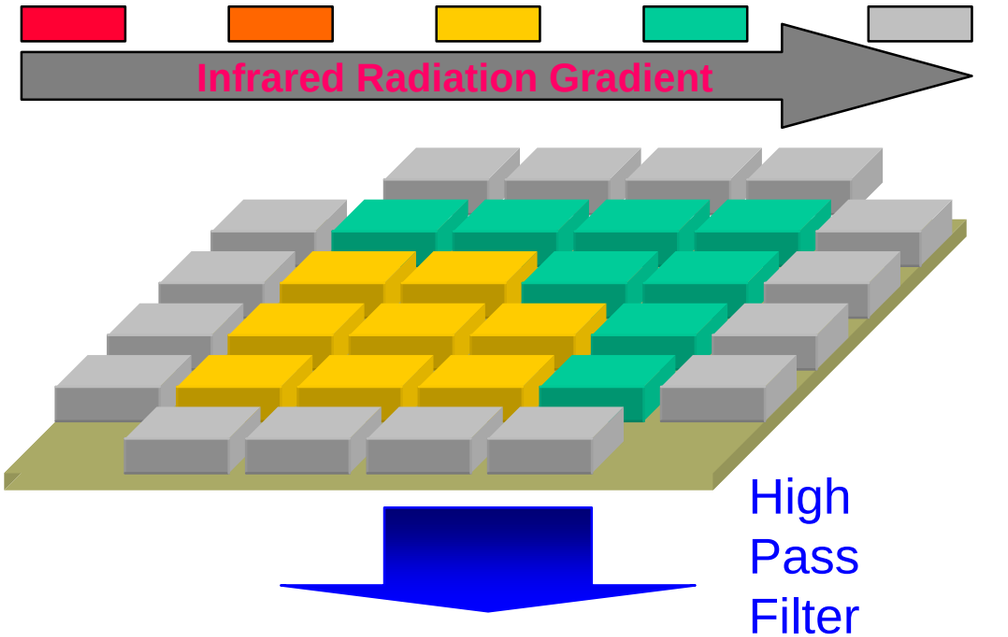
- The pixel processor has 8 functions:
  - shutdown
  - single pixel quantization
  - horizontal / vertical edge motion detection
  - horizontal / vertical high pass filtering
  - horizontal / vertical low pass filtering



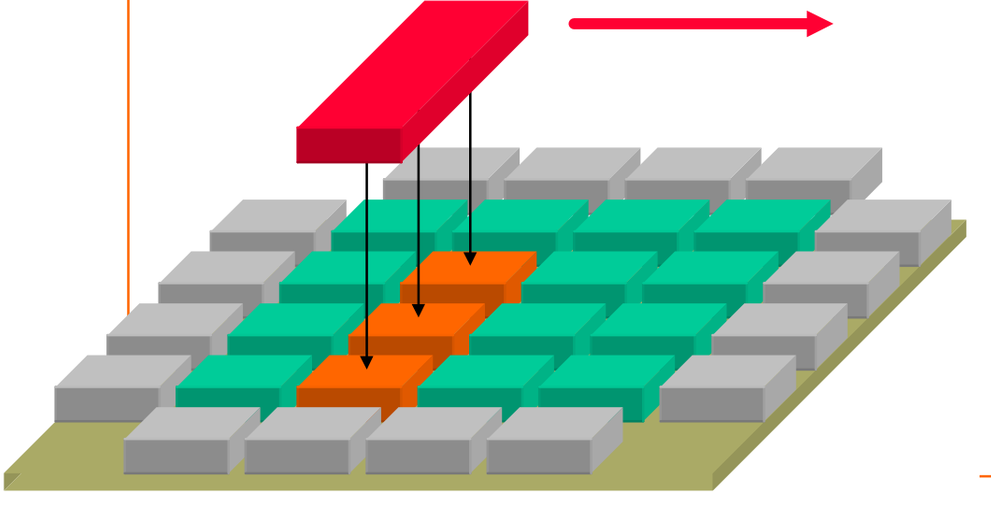
Source Motion Detection/ Spatial Filtering



11 01 01 01 Digital Output



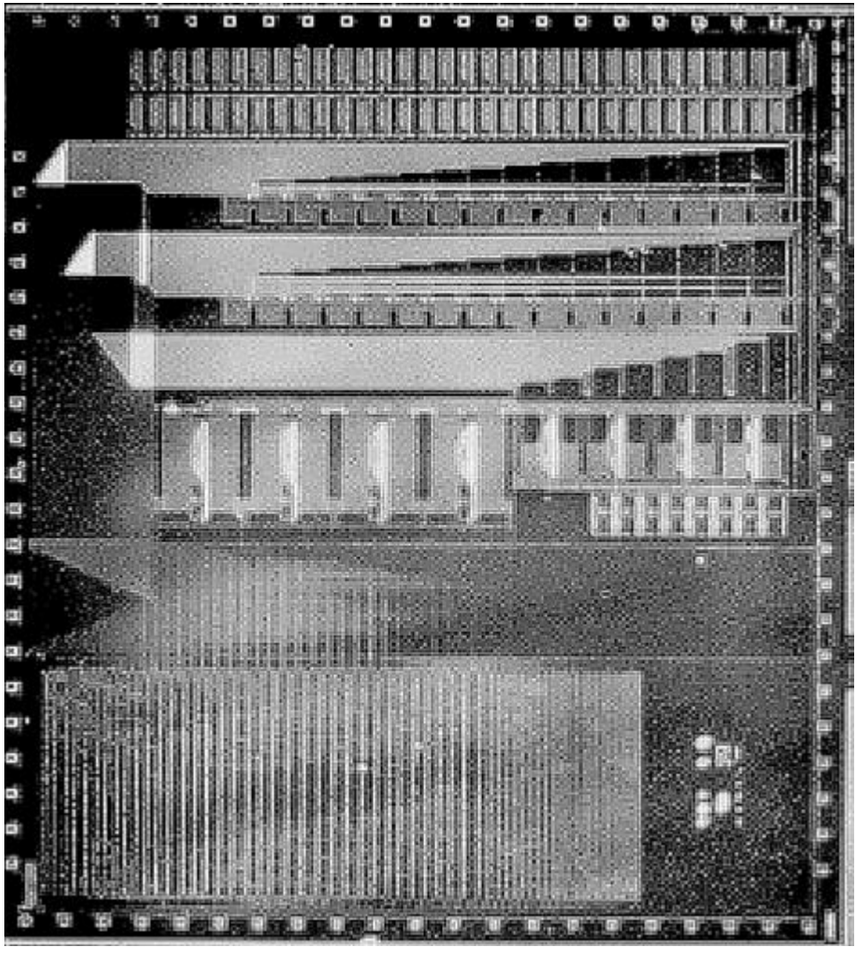
High Pass Filter



00 11 01 01 Digital Output

4	0	0	4
12	8	-8	4
12	0	8	-4
12	0	8	-4

IR Pixel Processor Layout



The 32 channel pixel processor is fabricated in 0.5µm HPCMOS.

The block level schematic illustrates the component placement of the pixel processor.

32 Preamplifiers

Bias

32 Element Variable Capacitor and Switch Array

4 Parallel Sigma-Delta Modulators with 8 Bit Resolution

4 Parallel OTAs

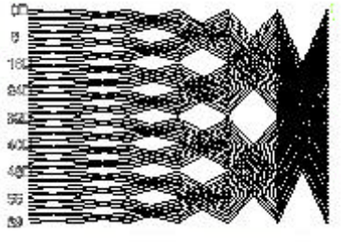
4 Parallel 2 Bit ADC

Sigma Delta Decimation Filters, Processor Control Logic, and Clock Generation

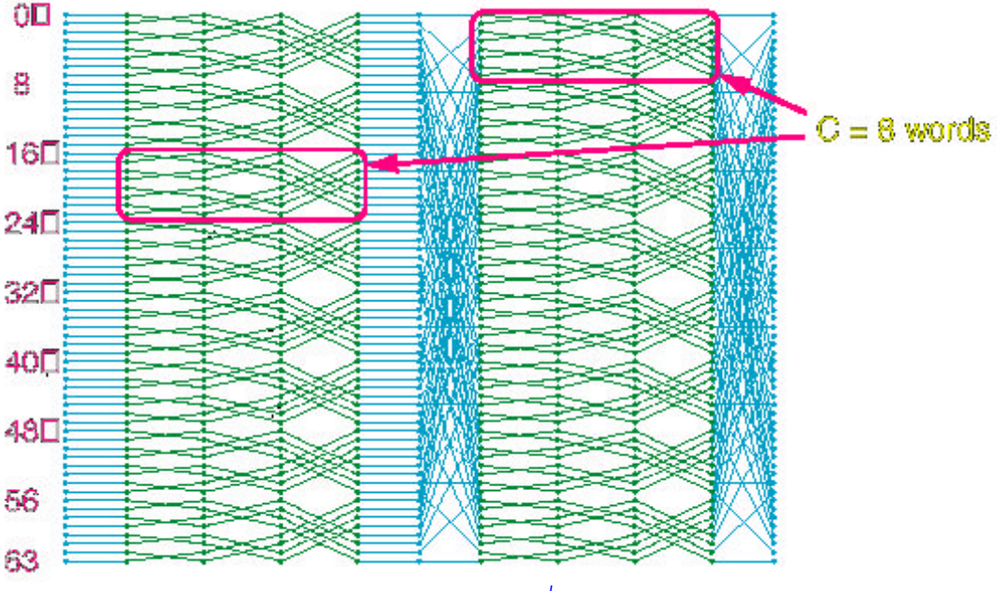
LWIM Spectrum Analyzer

- Continuous computation of tactical sensor power spectral density
- Scalable and programmable
- Cached-FFT Algorithm (B. Bass)

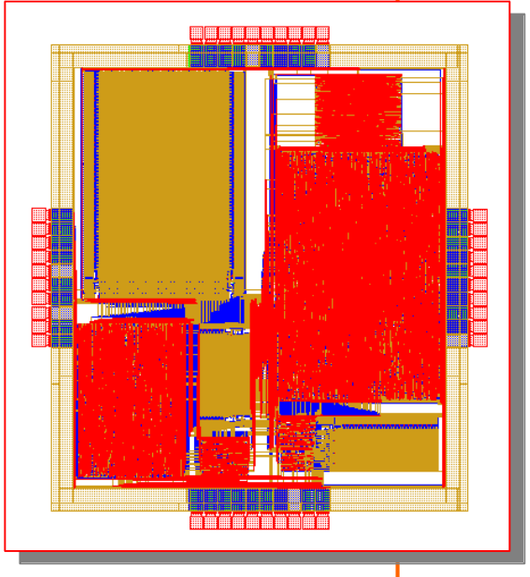
Standard FFT



Cached-FFT



Cache Size = √N
N= 64 => C= 8

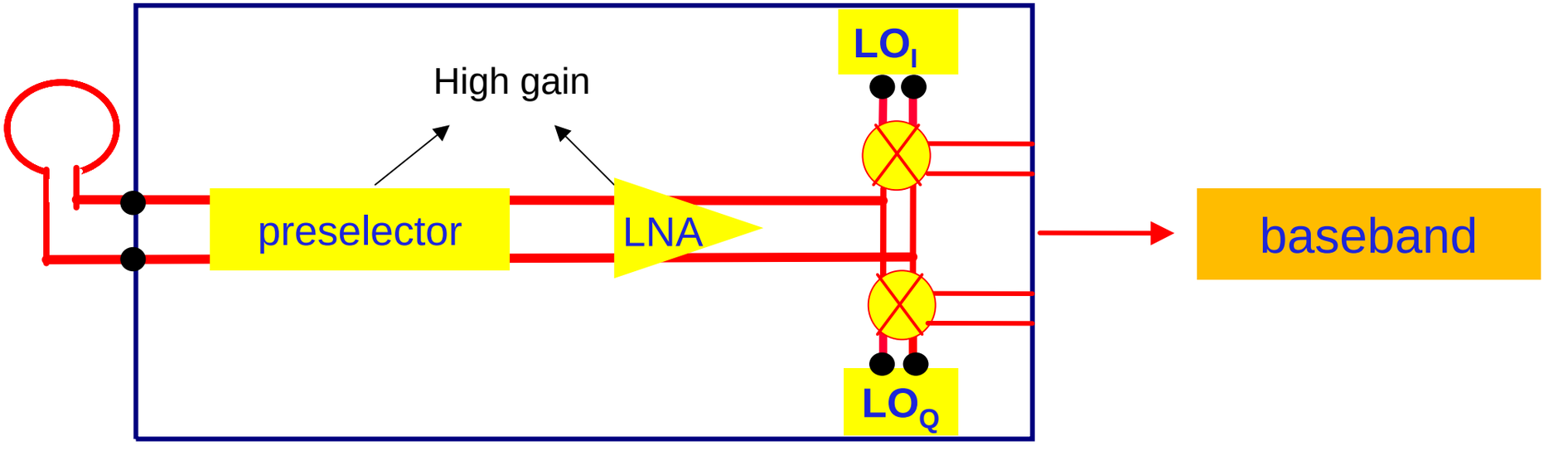


LWIM Comparison to Existing Wireless System

	Cellular	Bluetooth	LWIM
Noise Figure	8dB	Est (- 26)	~ 25dB
Sensitivity	-102dBm	-70dBm	~ -80dBm
Data rate	~10 kbps	1Mbps	≤ 100kbps
Current consumption	35 - 40mA	≤ 20mA	~ 1 mA

- Range and bandwidth reduction : *60 - 80dB gain in link budget*

Two Receiver Architectures

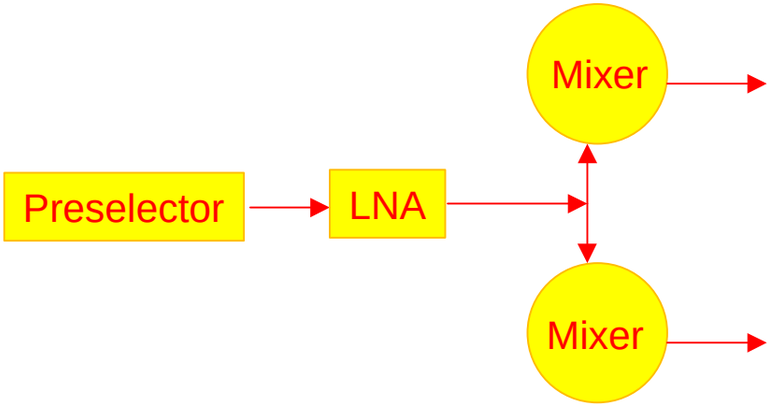


Goal: 1mA entire receiver system peak current drain

- High-Q inductive loads
- Off chip integration: LTCC components
- Two receiver architecture has been developed :
  - » Multi stage architecture: Preselector /LNA/Mixer
  - » Single stage architecture: Preselector/Combined LNA and Mixer

Two Architectures

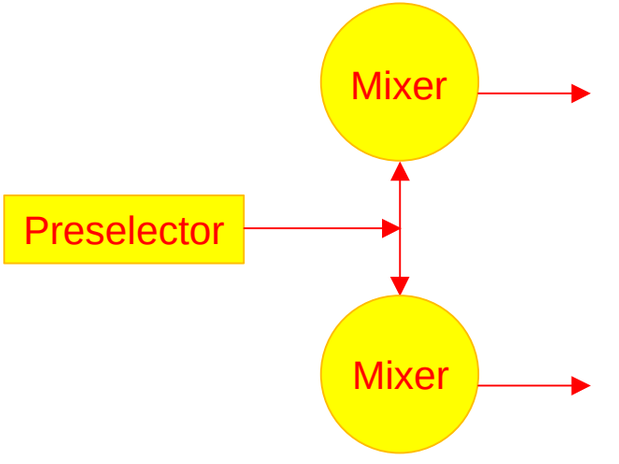
1 0.8 μm technology



Multi stage: Gain achieved by

- **Preselector:** High Q elements
- **LNA transistors gm**: Small due to the small current and relatively small transistor sizes
- **LNA output Impedance:** High Q components to generate large impedance at the output
- **Mixer input:** High impedance

2 0.6 μm technology

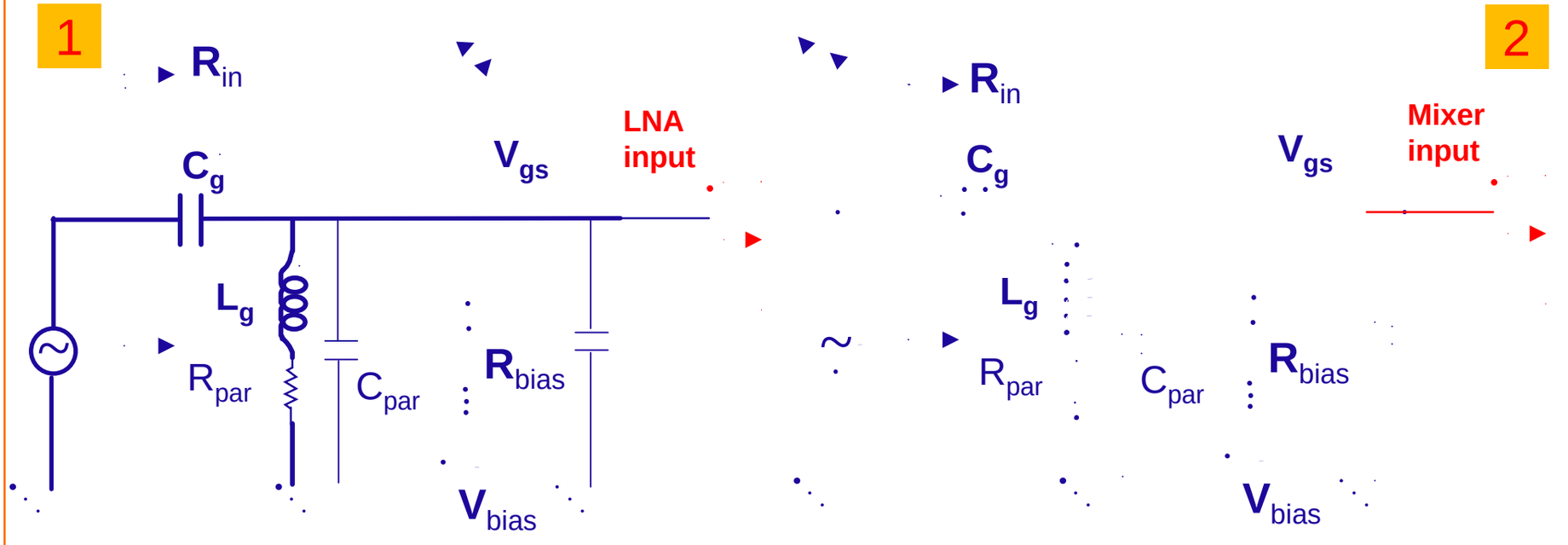


Single stage: Gain achieved by

- **Preselector:** High Q elements
- **Mixer transistors gm:** Small due to the small current and relatively small transistor sizes
- **Mixer output Impedance:** High impedance

Preselectors

Off-chip High-Q components



- ***Filtering***
- ***Matching***

  Choose L and C input impedance

  at ω_{res}**:**

- ***Gain from V_s to V_{gs}:***

$\omega_{res}=R_{bias}/\sqrt{L((C_g+C_{total})R_{bias}^2-L)}$

$R_{bias}\rightarrow\infty \quad \omega_{res}\approx 1/\sqrt{L(C_g+C_{total})}$

$R_{in}\approx L/R_{bias}(C_g \| C_{total})$

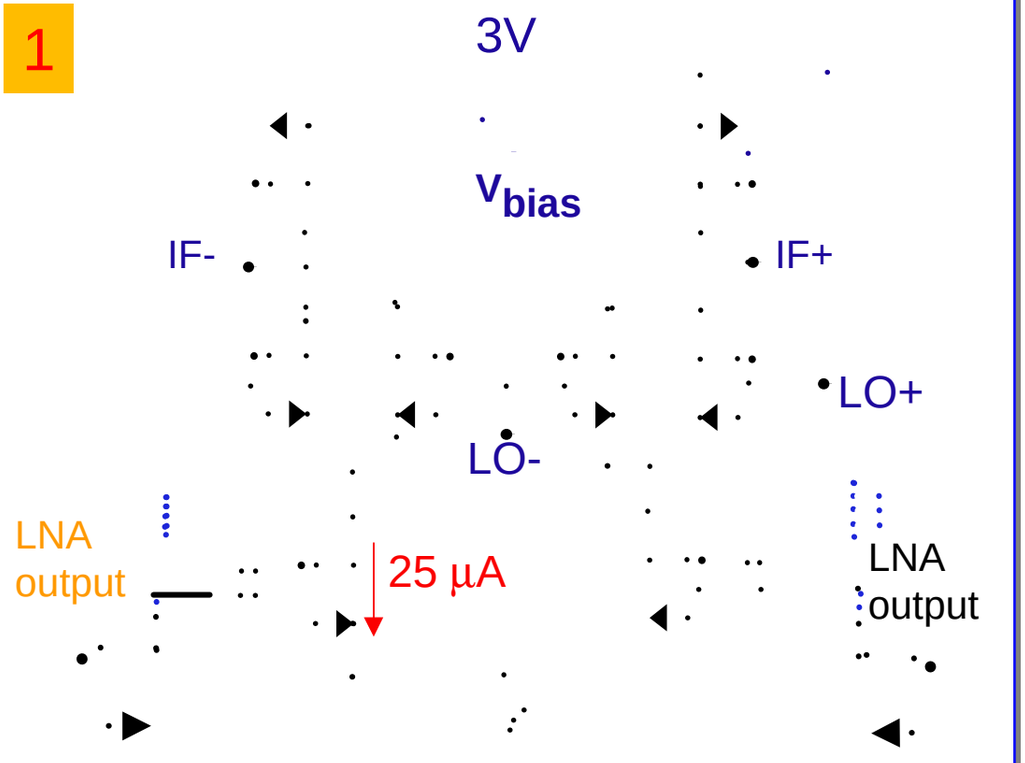
$V_{gs}/V_s \approx R_{bias}\sqrt{(C_g \| C_{total})/L}$

Passive

Mixers

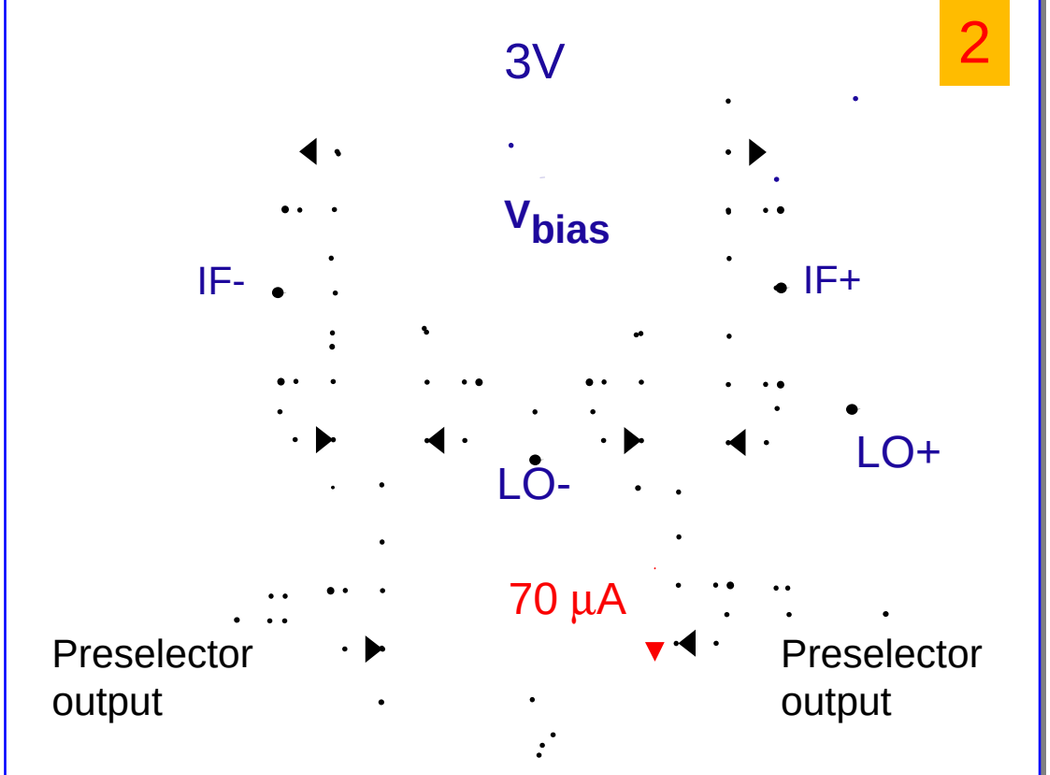
- Double-balanced Gilbert cell
- Direct conversion
- High output impedance
- Output bandwidth > 100 kHz

1



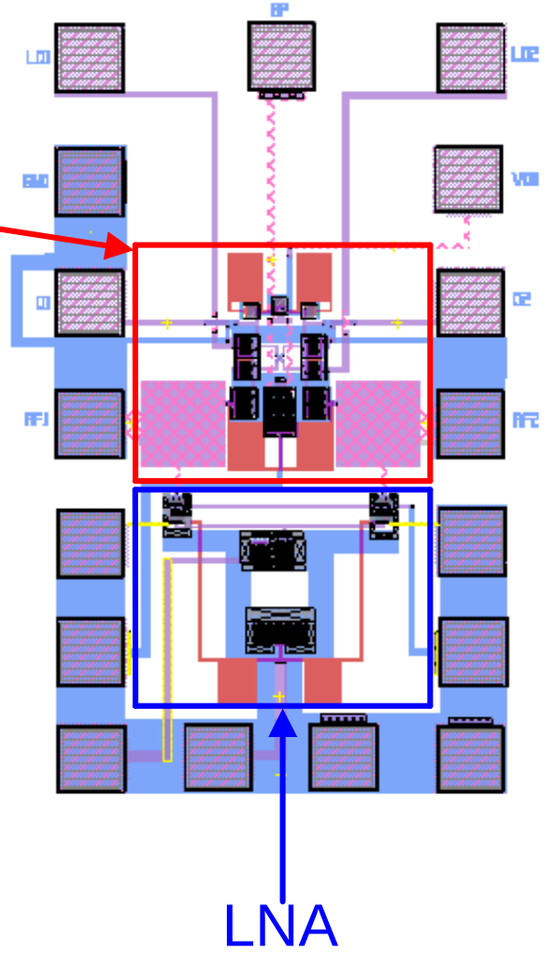
Total current drain = 110 µA

2

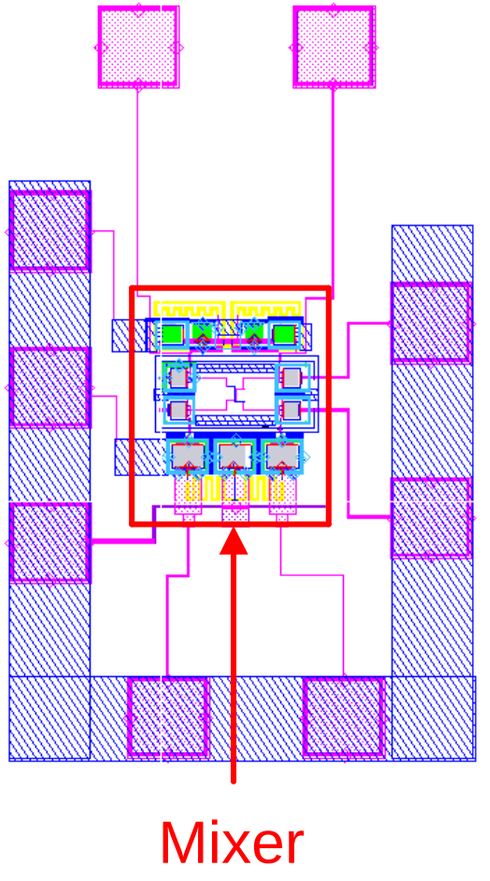


Total current drain = 140 µA

Receiver Front End

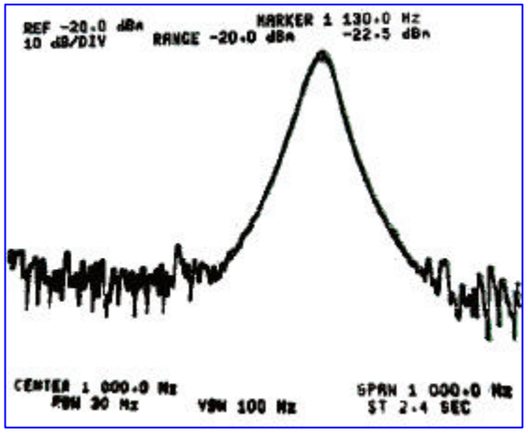
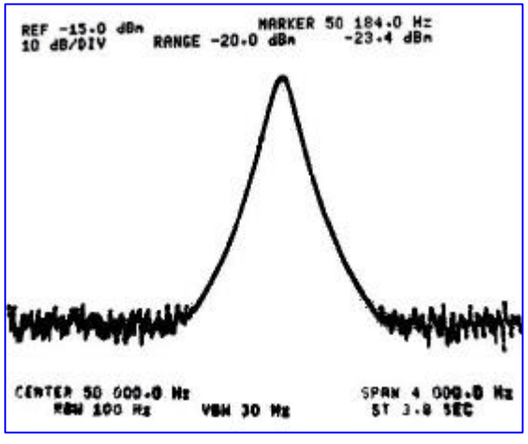
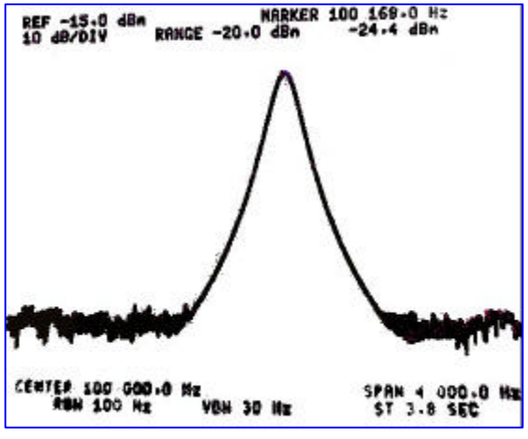
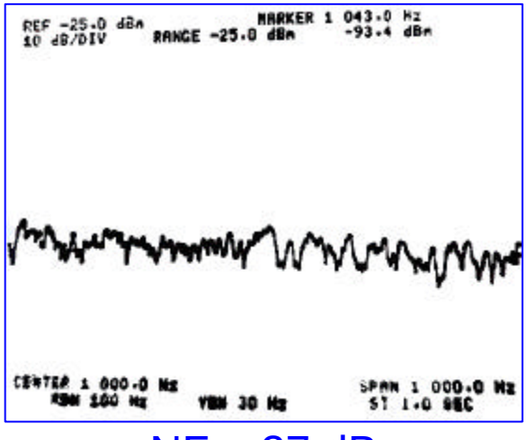
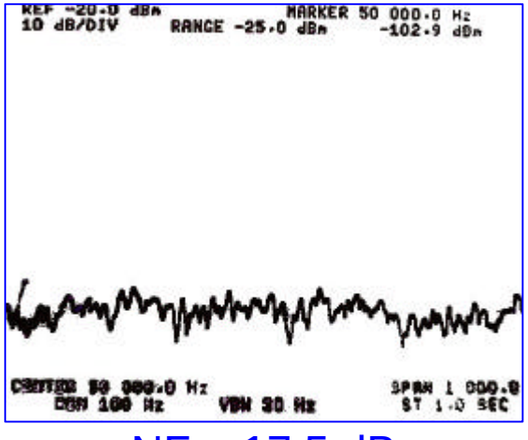
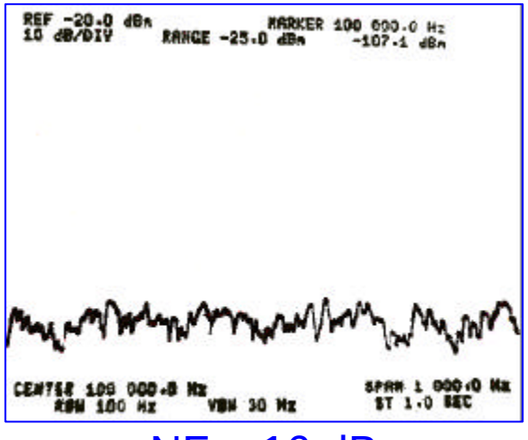


- Multiple stage architecture, 0.8 μm technology

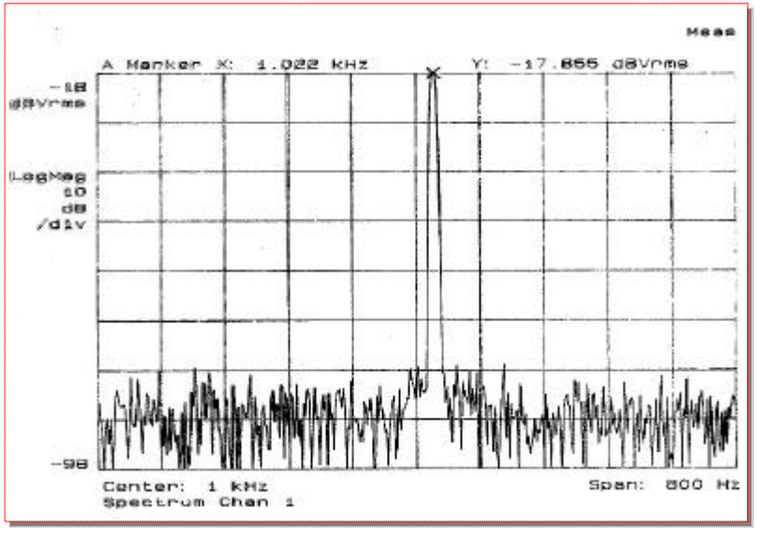


- Single stage architecture, 0.6 μm technology

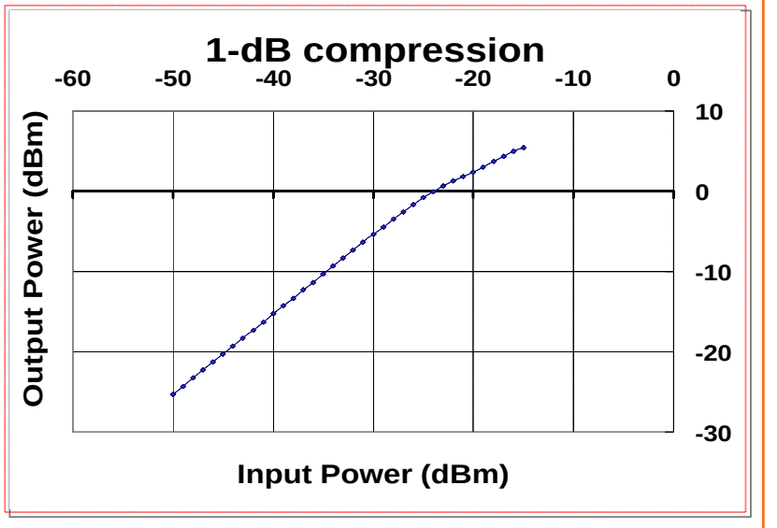
Gain / Noise for Single Stage

1 kHz	50 kHz	100 kHz
		
Gain = 30 dB	Gain = 29.5 dB	Gain = 29 dB
		
NF = 27 dB	NF = 17.5 dB	NF = 16 dB

Gain/Noise /1dB Compression for Multi Stage

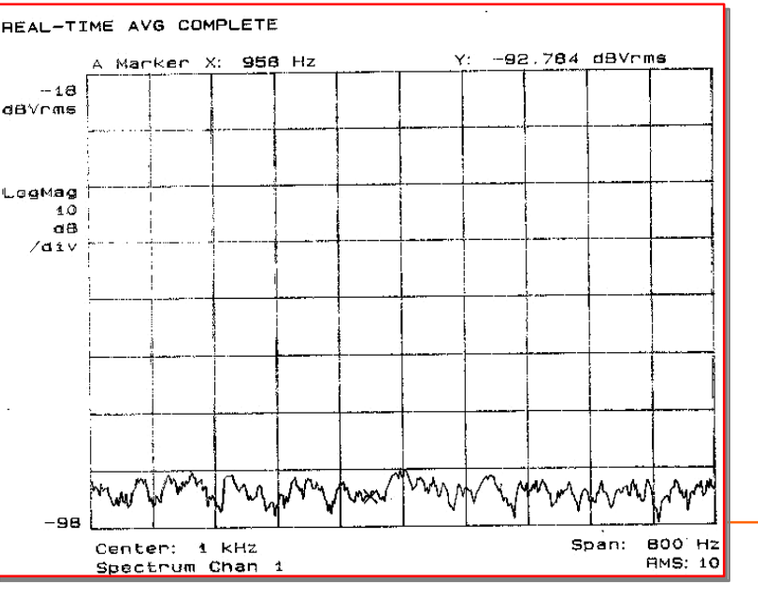


LNA input = -43dBvrms
Mixer output = -17.85dBvrms
Gain = 25 dB



1-dB compression at -25dBm
(effective power)

This front-end:
At 1KHz: NF ≈ 28dB
At 25KHz: NF ≈ 19.5 dB



IF Frequency Dependence

- Multi-stage Architecture (0.8 μm)

	@1 khz	@25 khz
Gain	25 dB	24 dB
NF	26 dB	19.5 dB
IP3	-15 dBm	-15 dBm
1 dB	-25 dBm	-25 dBm

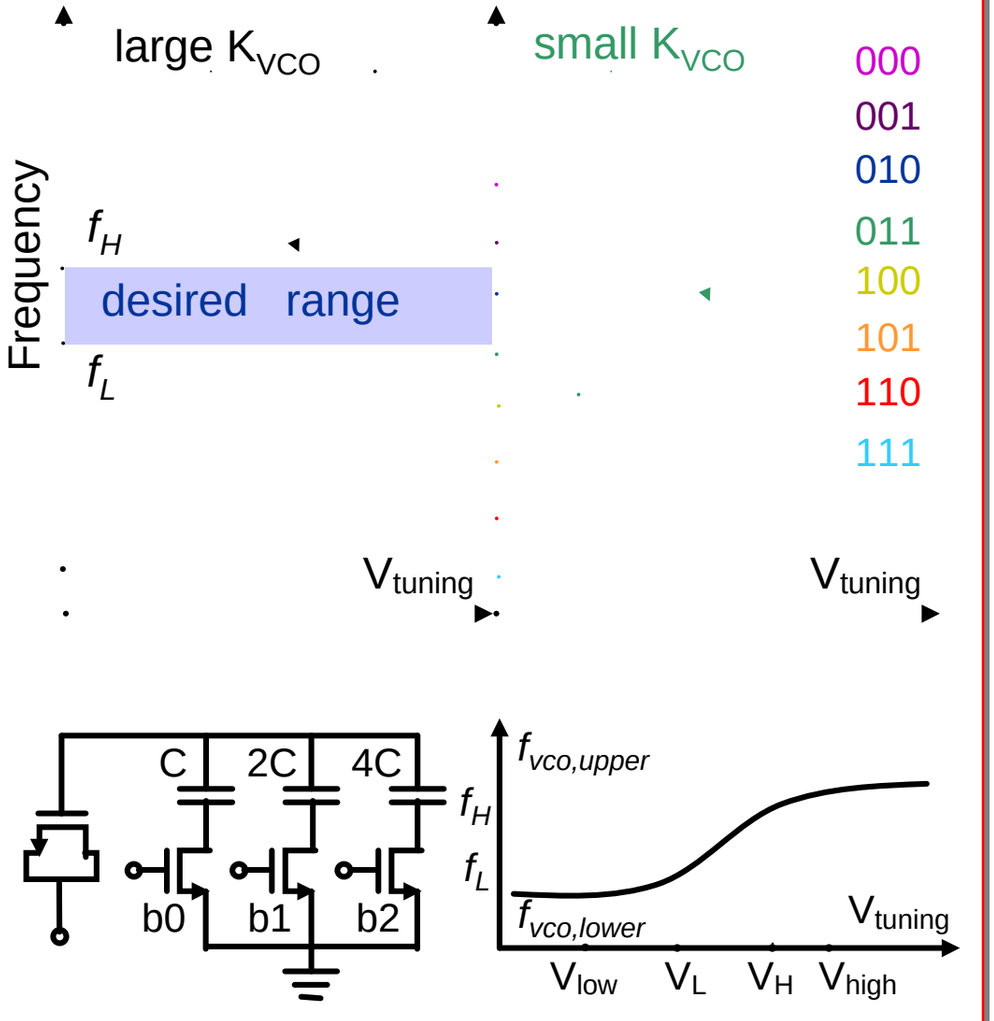
- Single-stage Architecture (0.6 μm)

	@1 khz	@25 khz
Gain	30 dB	30 dB
NF	27 dB	21 dB
IP3	-13 dBm	-13 dBm
1 dB	-23 dBm	-23 dBm

Frequency Synthesizer Design

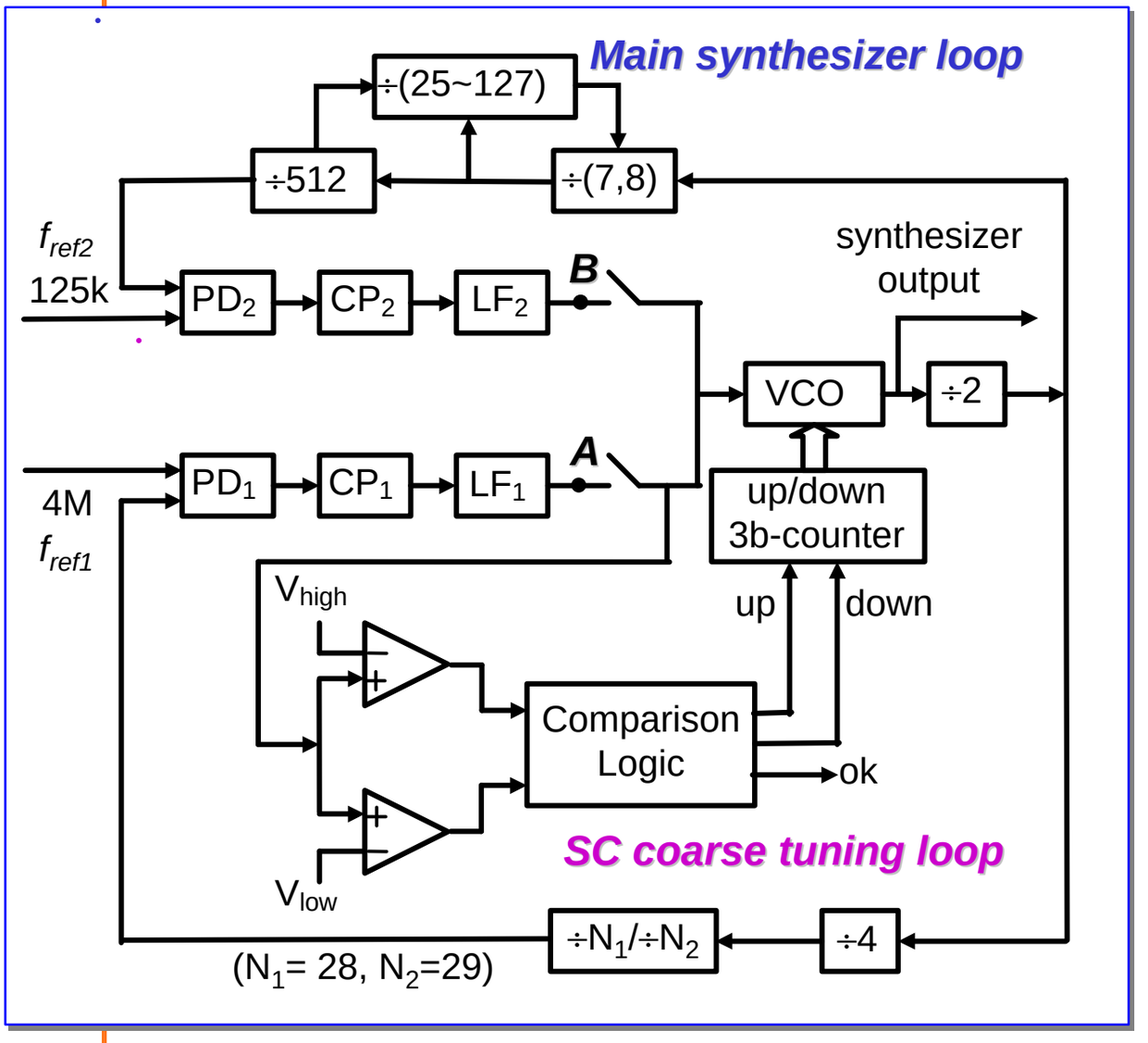
- **Frequency synthesizer requirements:**
  - switching time: less than 2 msec is adequate for typical wireless sensor applications (latency tolerant)
  - frequency resolution: 250/500 kHz
  - low power operation: < 1.5 mA drain current
- **Frequency synthesizer techniques:**
  - direct digital frequency synthesizer: fast switching, fine frequency resolution, but very high power
  - PLL: complex tradeoffs among frequency resolution, switching speed, and spurs; possible low power solution
- **PLL architecture choice:**
  - integer-N architecture: wide channel spacing and relaxed switching time requirements permit this low power PLL architecture

Wide Tuning Range and Low Noise



- minimize K_{VCO} by breaking a wide-range tuning curve into several narrower-range tuning curves
  - » require continuous and discrete tuning elements
- continuous tuning: CMOS varactor
- discrete tuning: select L or C
  - » choose C, mature for CMOS implementation
  - » binary-weighted SC tuning
- require an auxiliary loop in the PLL to automatically search for the proper switch state
- searching algorithm is based on frequency comparison
  - » This is done by comparing voltage quantity!

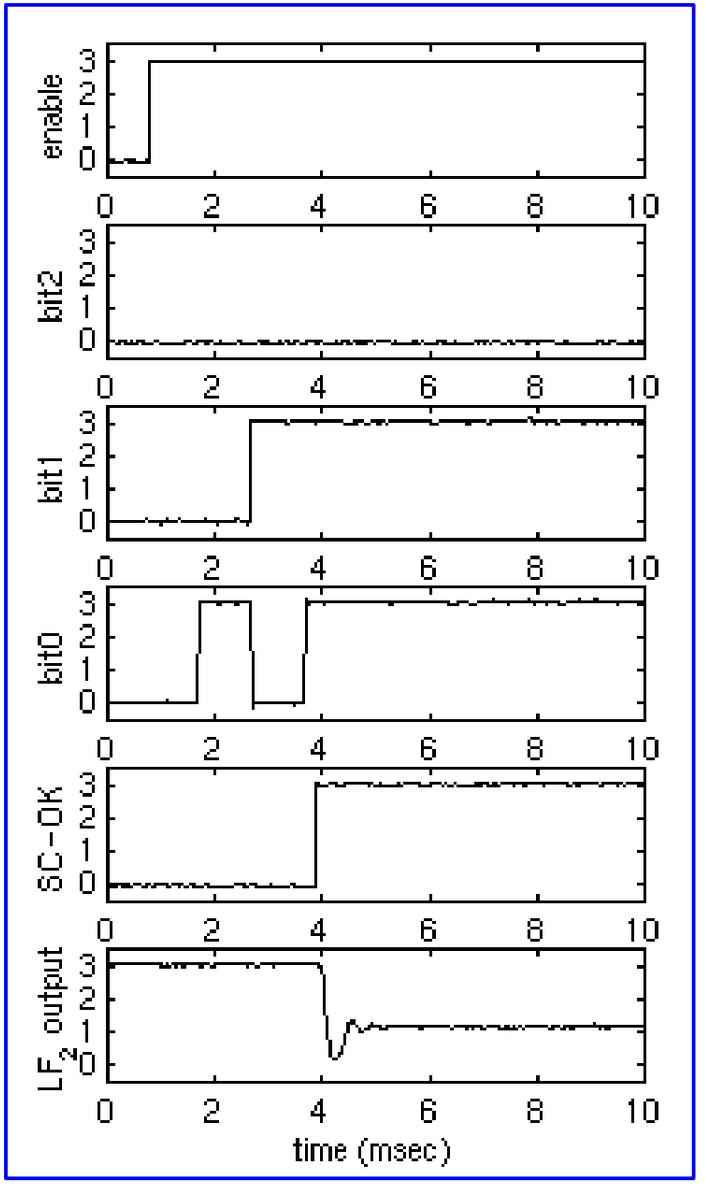
PLL with SC Coarse Tuning Loop



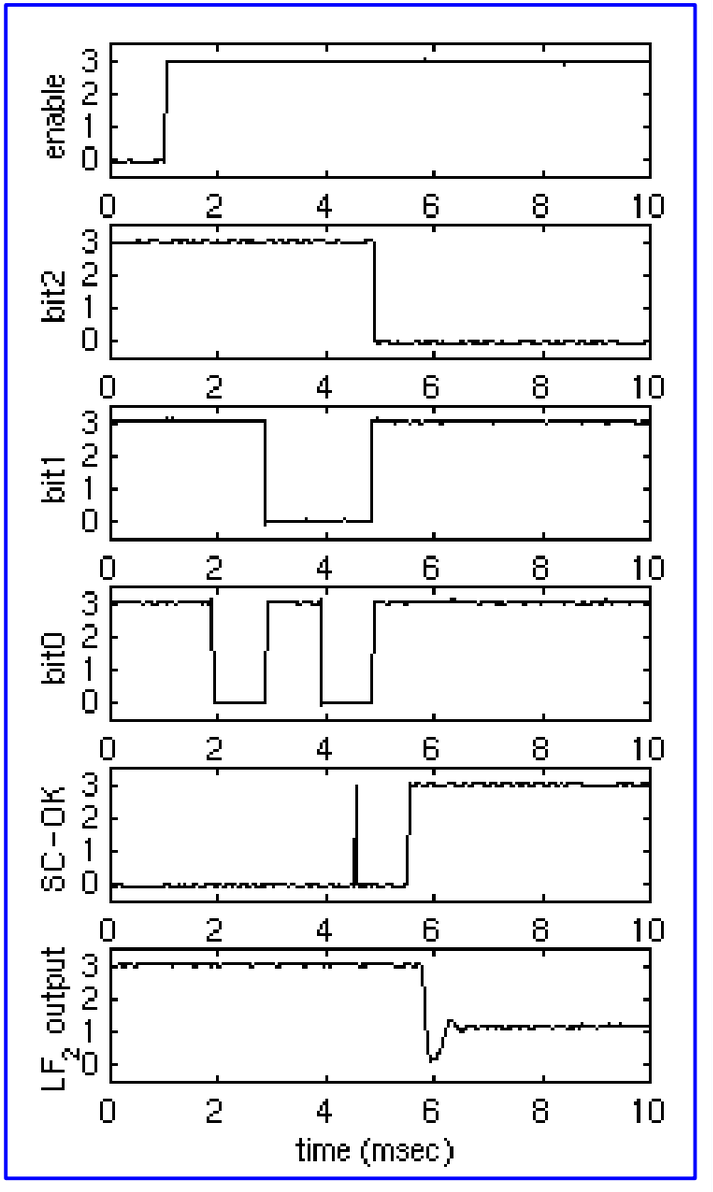
Example: assume f_L=902, f_H=928 MHz

- VCO (@111) < 902 & 928
  - Þ tuning voltage → V_{DD}
  - ⇒ comparison stage → down
  - ⇒ 111 → 110, C↓
  - ⇒ VCO → higher frequency
- VCO (@000) > 902 & 928
  - ⇒ tuning voltage → V_{SS}
  - ⇒ comparison stage → up
  - ⇒ 000 → 001, C↑
  - ⇒ VCO → lower frequency

Measurement Results



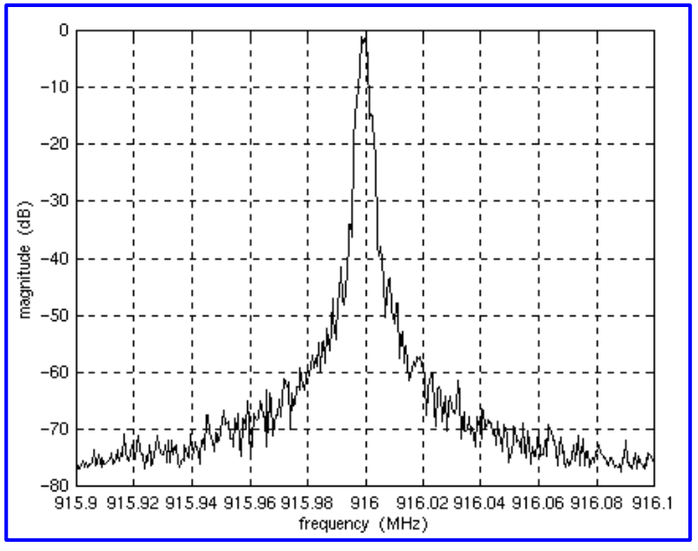
(a) 000 → 011



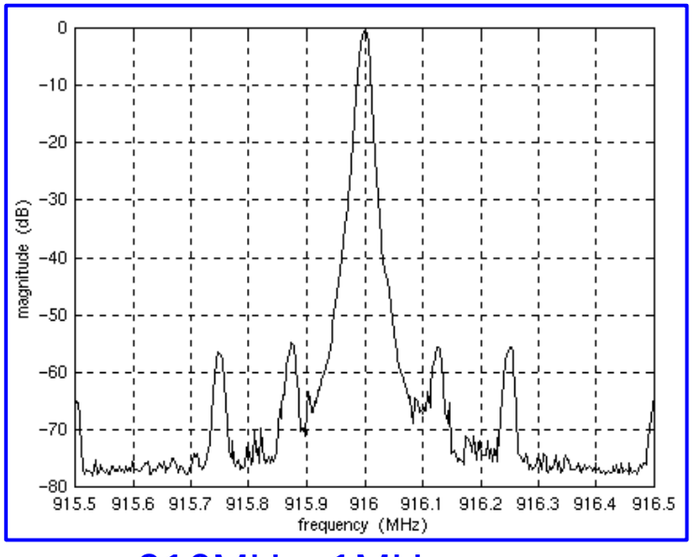
(b) 111 → 011

- Complete PLL operation

Measurement Results

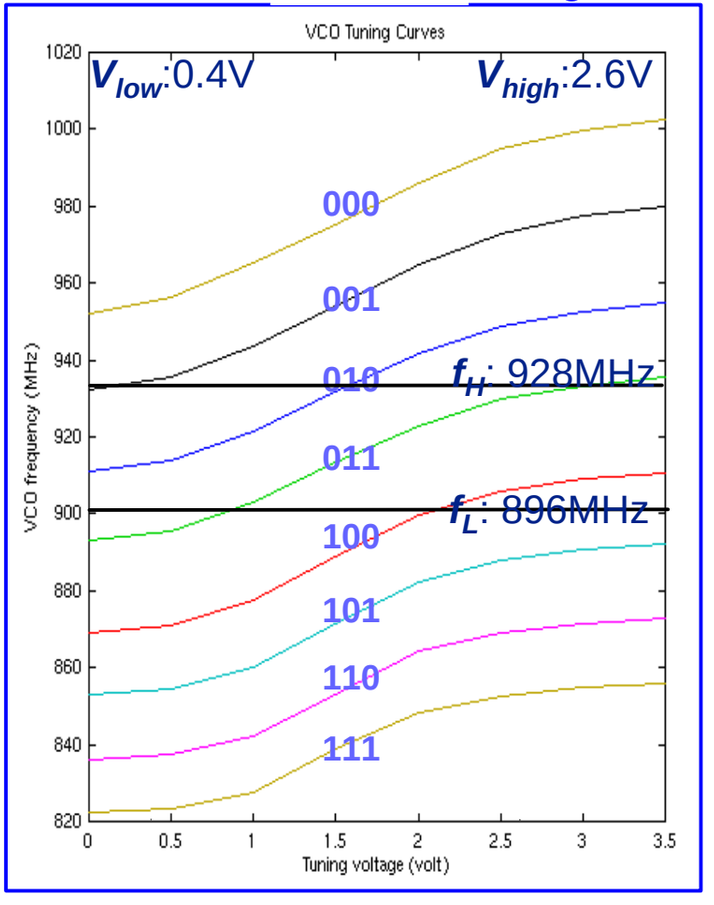


916MHz, 200kHz span (RBW:1kHz)



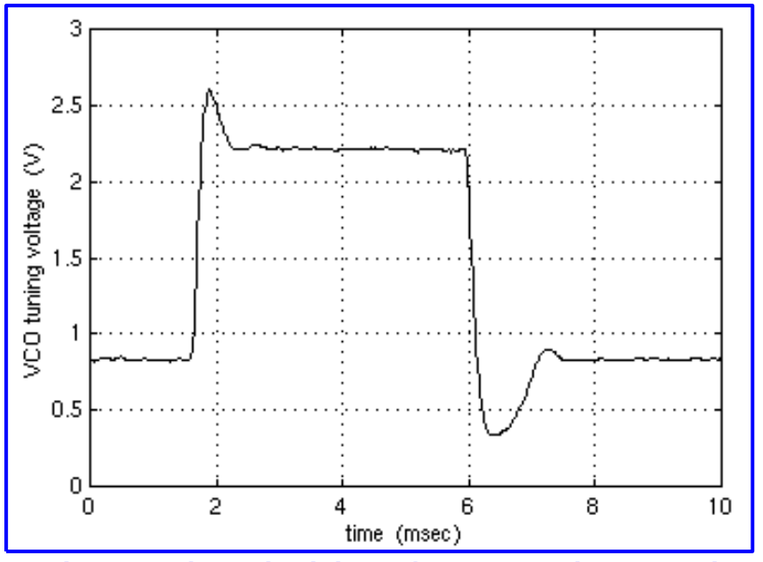
916MHz, 1MHz span

Measured VCO tuning

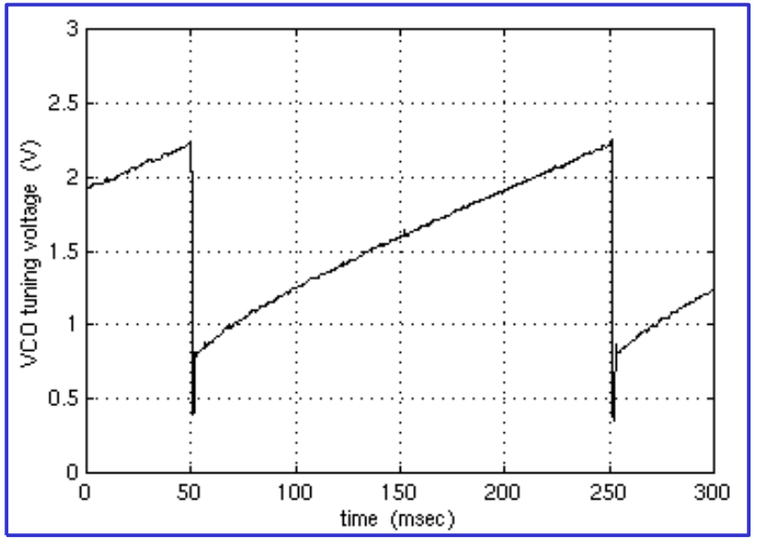


- VCO gain: 20MHz/V
- overall tuning range: ~20% (180MHz)
- spur: -55dBc
- phase noise: -102dBc/Hz @100kHz

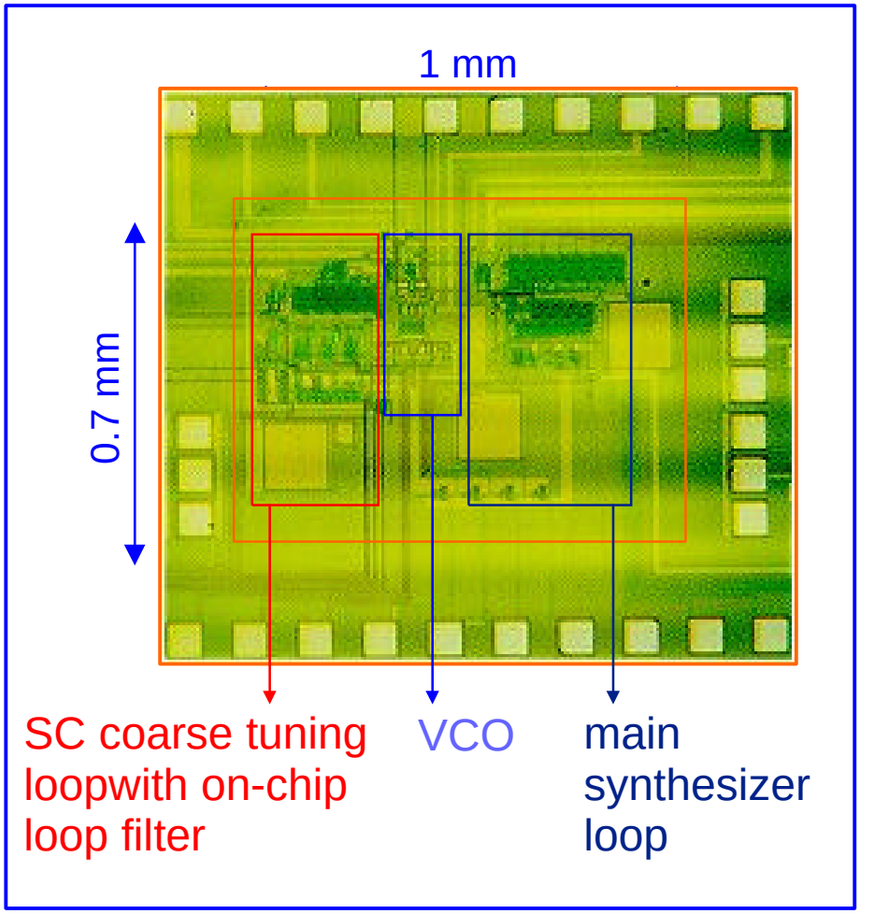
Measurement Results



channel switching from end to end

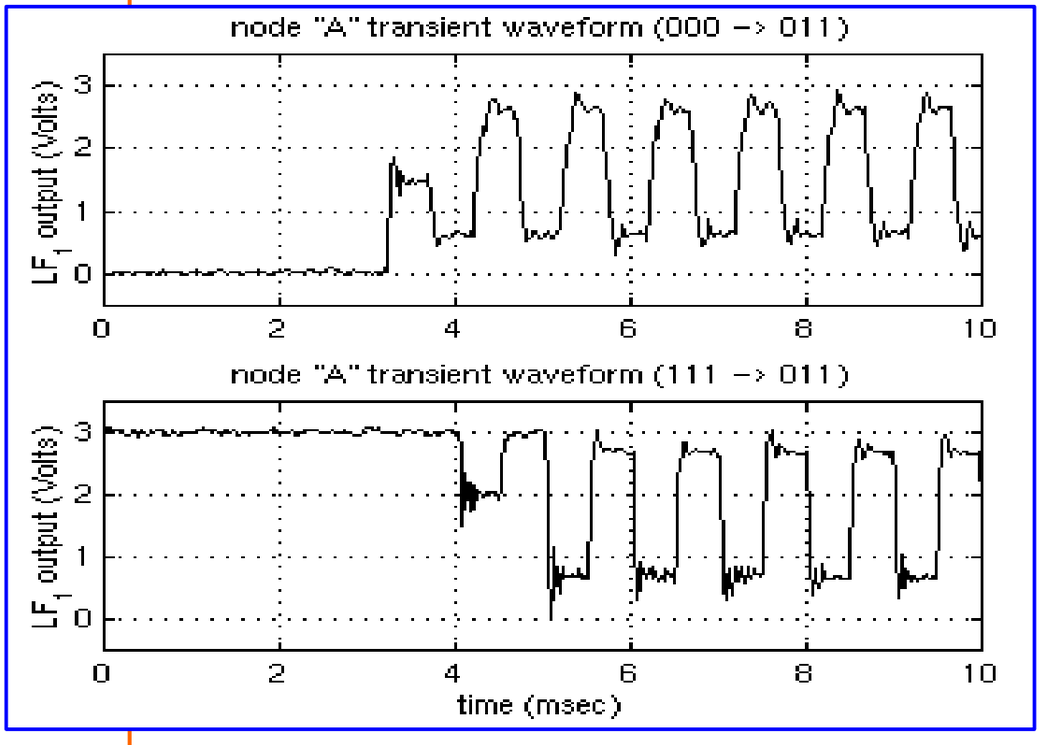


frequency hops across the ISM band

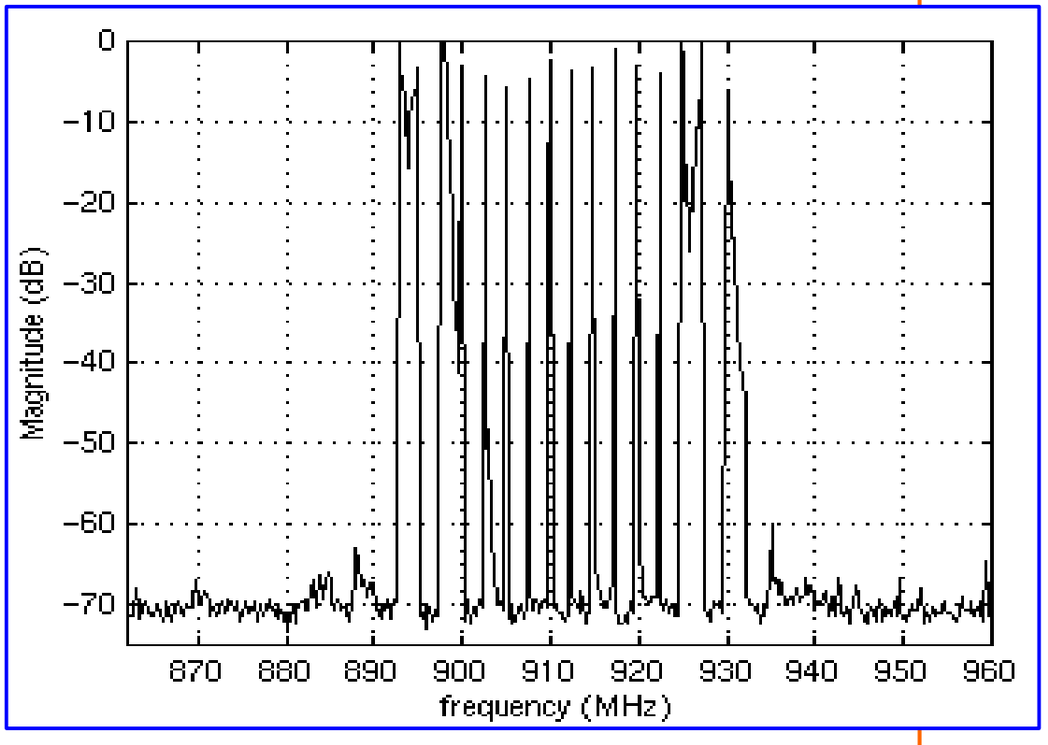


- switching time ~ 2msec
- 0.6 µm CMOS technology
- total current: 2.5mA (2.2mA with SC loop disabled)

Measurement Results: SC Loop



tuning waveforms at the LF_1 output



SC loop output spectrum at the 'ok' state

- the SC loop at the 'ok' switch state will lock the VCO to 896 and 928 MHz periodically

LWIM LTCC Integration

- **LTCC: Low Temperature Co-fired Ceramic**
  - low loss substrate
  - high quality RF passives
  - microsensor integration