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CMOS Front-End for Micropower RF Wireless System

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UCLA Electrical Engineering

WINS

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Outline

- Introduction to Wireless Integrated Network Sensors (WINS) Project: Network, Applications, Nodes
- Unique Transceiver Requirements
- RF Architecture:
  - **Receiver:** Preselector, LNA , Mixer, VCO and PLL Architecture
  - **Transmitter:** PA Architecture
- Future work: (WINS integration)
- Summary

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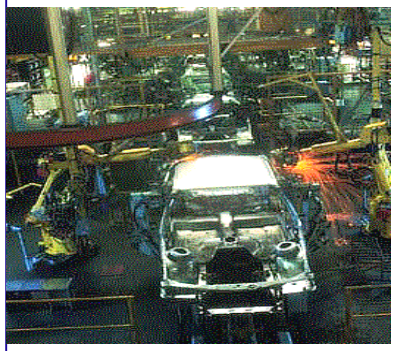
Wireless Integrated Network Sensors (WINS)

- Low-power Networking

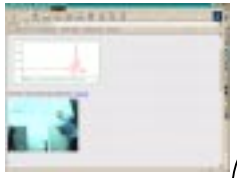
Medical instrument internetworking



Industrial controls

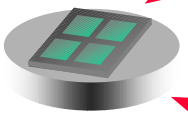
Consumer

worldwide user

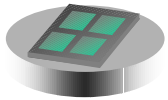


Internet

networking



sensing



signal processing

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Network Characteristics

- Dense node distribution
- Short range (<30m)
- Low bit rate (<100kbps) typical sensors systems are band limited
- Latency tolerant
- Compact cell
- 3 years life
- 100 μW average
- 3mW peak

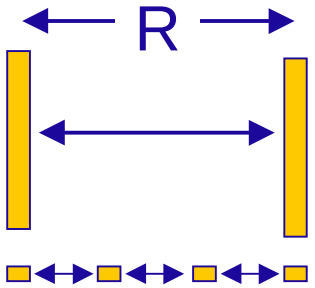
Implement multihop for power reasons:

RF path loss:

$$P \propto \frac{1}{R^{\alpha}} \quad (\alpha \approx 3-5)$$

Relative system power advantage for N-hop chain:

$$\frac{P_{total}(N)}{P_{total}(1)} \propto \frac{1}{N^{(\alpha-1)}}$$



multihop

WINS Communication Requirements

- In the design of WINS communication system must consider:
  - Stringent power limitation ⇒ low power architecture
  - wireless microsensor applications ⇒ reduced data rate
  - Multihop network operation ⇒ node-to-node link budget is relaxed

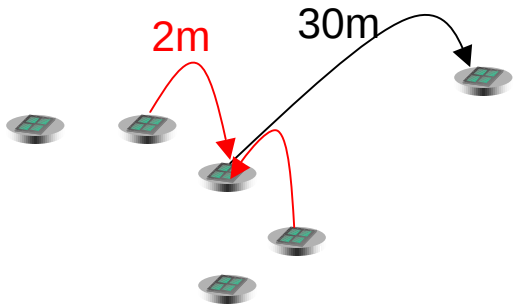
	Specs	Extension
Operation frequency	ISM band (902-928 MHz)	2.4 GHz
Modulation scheme	binary FSK	4-FSK
Channel spacing	500 kHz	250 ~ 500 kHz
Tone frequency	100 kHz	60 ~100 kHz
Data rate	10 kbps	1 ~ 100 kbps
Frequency Accuracy	20 ppm	< 30 ppm
Transmission power	-10 ~ 10 dBm	nominal: 0 dBm
SNR required	< 10 dB (BER: 10e-3)	TBD
Hopping rate	100 hops/sec	TBD

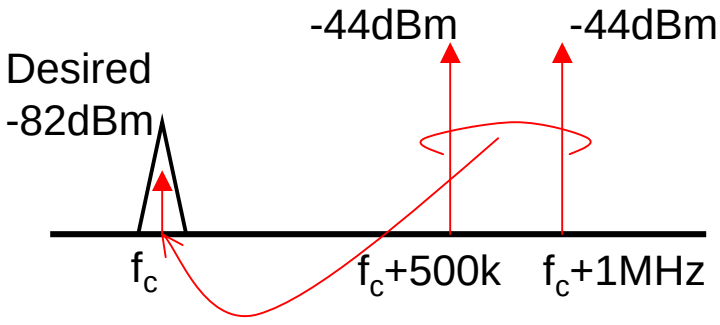
WINS Communication Approaches

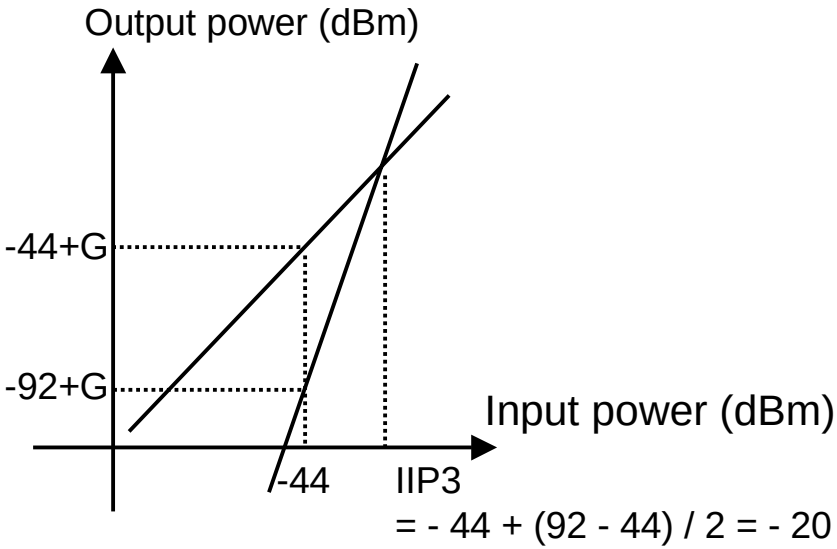
- Signaling: FSK
  - allow power-efficient non-linear PA
  - allow low power modulation and demodulation circuitry
  - spectrum efficiency is not a main concern in most microsensor applications
- FSK Tone Frequency: 100kHz
  - To minimize the impact of baseband *1/f* noise and account for the inaccuracy of reference frequency source (20 ppm), the FSK tone frequency is chosen to be 100 kHz, independent of data rate.
- Channel Spacing: 250-500kHz
  - 250 ~ 500 kHz; lower bound is set by the baseband channel-select filter design (avoid sharp transition from passband to stopband), upper bound is set by FCC regulation (at least 50 hopping channels are required)
- Path Loss:
  - assume n=4, d=30 m $\Rightarrow$ maximum path loss ~ 92 dB
- Sensitivity (MDS, desired minimum detectable signal):
  - MDS = 10 dBm (maximum transmitting power) -92 dB (path loss) = -82 dBm

WINS Communication Approaches

- Noise Figure:
  - NF = 174 - $10\times\log_{10}$BW - SNR_{min} + MDS - 5 dB (margin) = 25 dB
- Linearity (IIP3):
  - With simple power control scheme and proper nodes distribution, the two-tone interfere is at -44 dBm; the IIP3 is calculated to be -16 dBm (with 4dB margin).
  - 2nd-order distortion (IP2) is mitigated by differential circuit architectures







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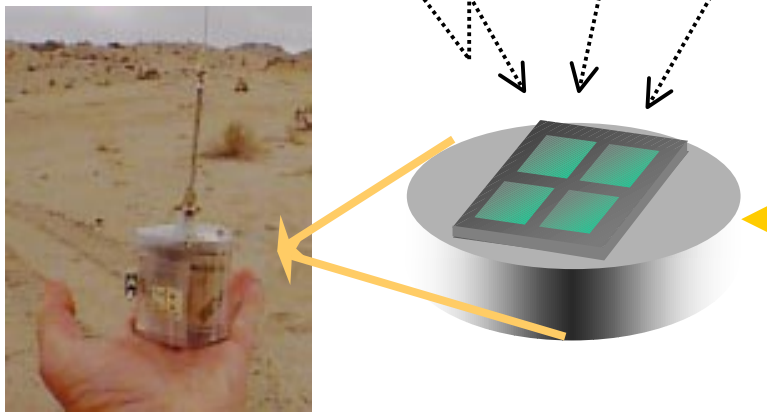
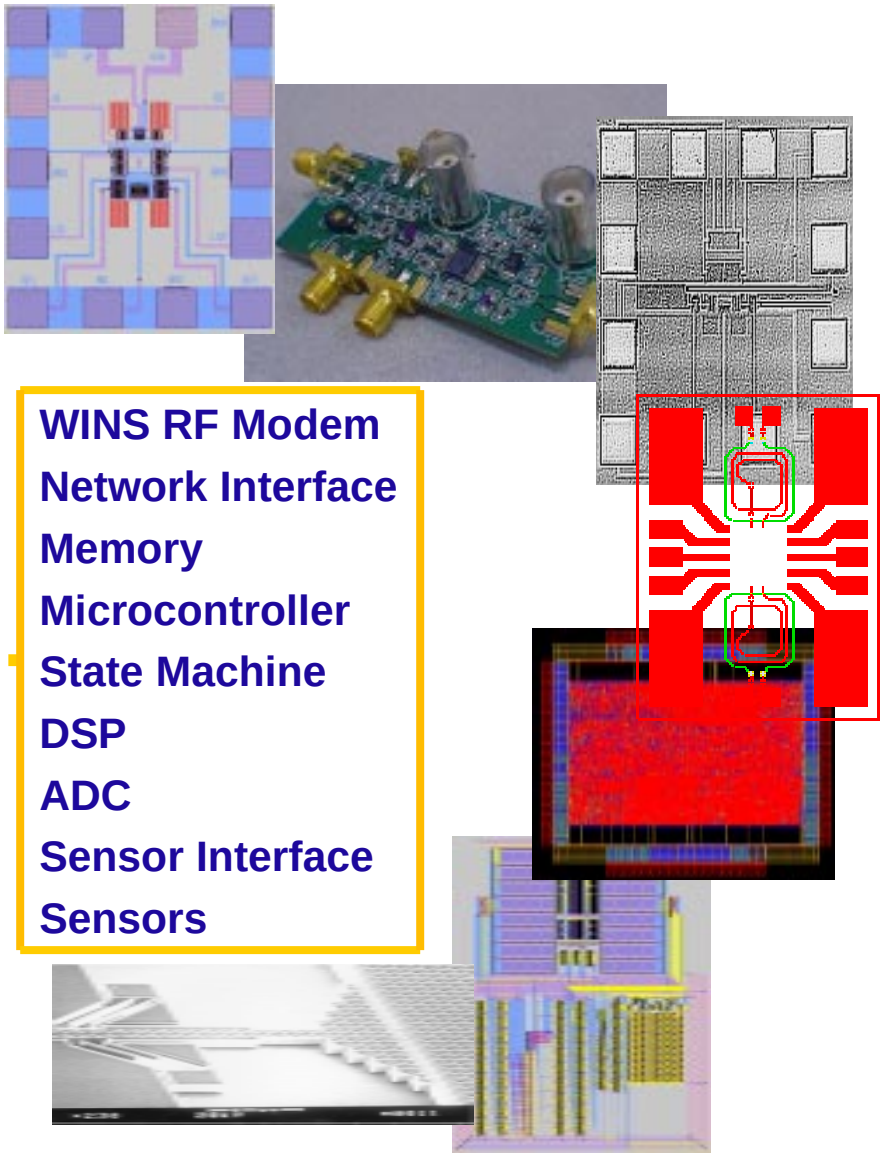
WINS Nodes





- WINS RF Modem
- Network Interface
- Memory
- Microcontroller
- State Machine
- DSP
- ADC
- Sensor Interface
- Sensors

WINS

WINS vs. Existing Wireless System

Characteristic	Wireless LAN	Cellular Telephony	WINS
Range	~ 200m	~ 5km	≤ 30m
Data Throughput	~ 2-10Mbps	~ 10kbps	≤ 100kbps

Conclusions:

- **Range and bandwidth reduction : *60 - 80dB gain in link budget***

Why Design a New Receiver?

- Performance specifications of receivers:

	Cellular	Bluetooth	WINS
Noise Figure	8dB	Est (- 26)	~ 25dB
Sensitivity	-102dBm	-70dBm	~ -80dBm
Data rate	~10 kbps	1Mbps	≤ 100kbps
Current consumption	35 - 40mA	≤ 20mA	~ 1 mA

- Challenge: Minimum noise figure and best sensitivity for long range communications.
- Specifications of the front-end receiver for WINS project:

  Digital CMOS transistor
  Current consumption ≤ 200 μA
  Gain ≅ 20 - 25dB
  Noise figure ≅ 20 dB

- Challenge: Micro power for short range communications (30 m)

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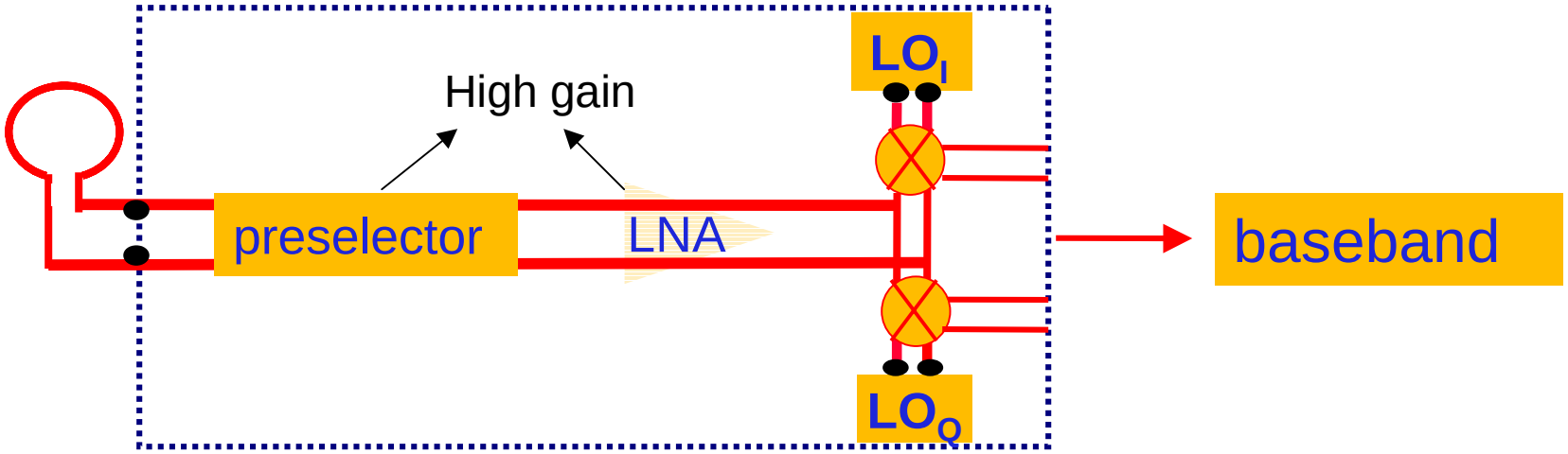
WINS

Two Examined Receiver Architectures



Goal: 1mA entire receiver system peak current drain

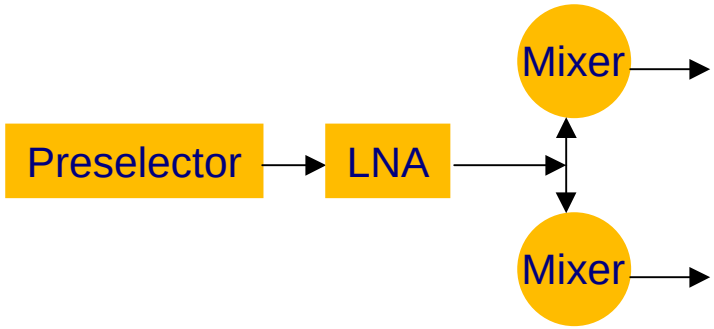
- High-Q inductive loads
- Off chip integration: LTCC components

Two receiver architecture has been developed :

- Multi stage architecture: Preselector /LNA/Mixer
- Single stage architecture: Preselector/Combined LNA and Mixer

Two Architectures

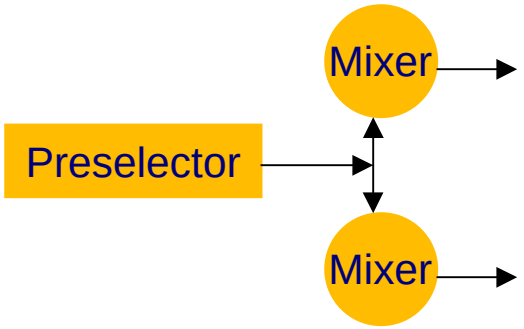
1 0.8 μ technology



Multi stage: Gain achieved by

- **Preselector:** High Q elements
- **LNA transistors gm**: Small due to the small current and relatively small transistor sizes
- **LNA output Impedance:** High Q components to generate large impedance at the output
- **Mixer input:** High impedance

2 0.6 μ technology

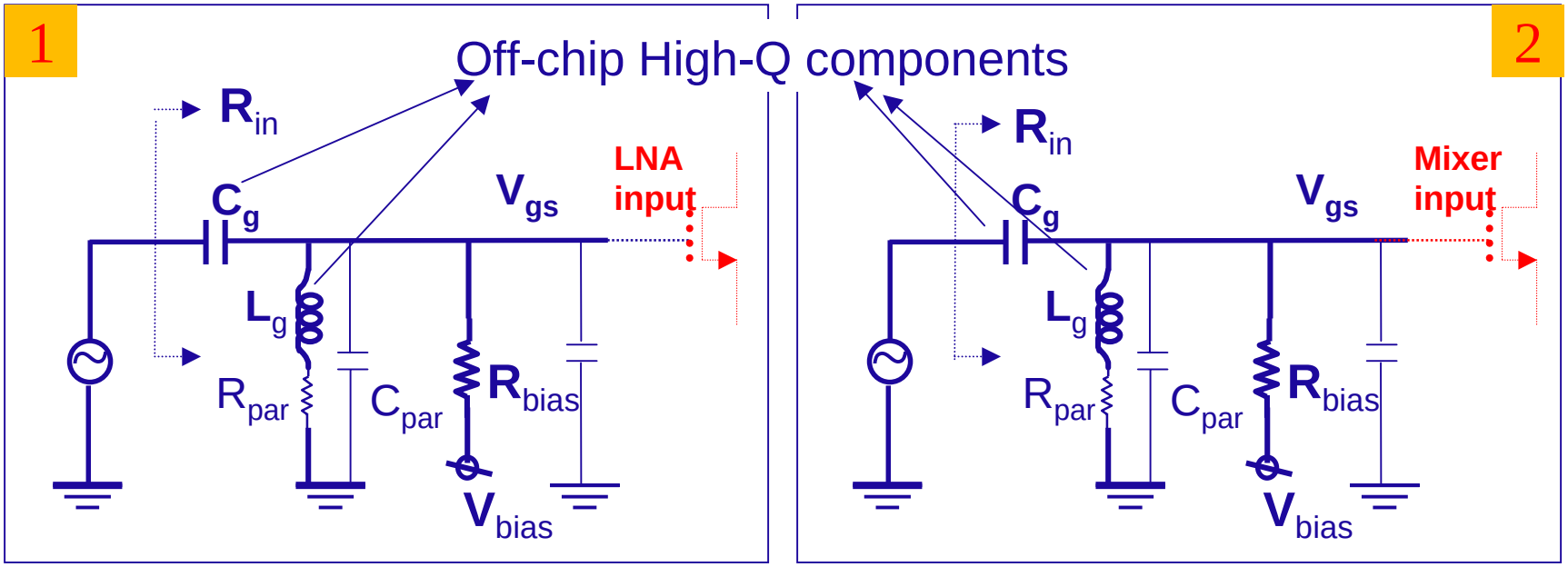


Single stage: Gain achieved by

- **Preselector:** High Q elements
- **Mixer transistors gm:** Small due to the small current and relatively small transistor sizes
- **Mixer output Impedance:** High impedance

Mixer is the only current user stage! ⇒ Gain and less NF

Preselectors



- **Filtering**
- **Matching** Choose L and C

input impedance at ω_{res}: →

- **Gain from V_s to V_{gs}:**

$$\omega_{res} = R/\sqrt{L((C_g + C_{total})R^2 - L)}$$

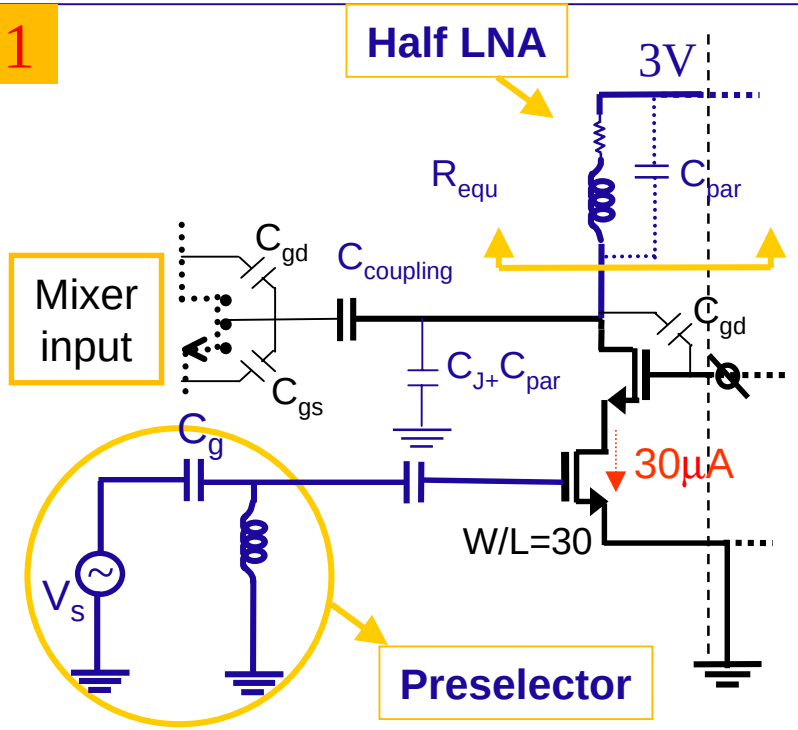
$$R \to \infty \quad \omega_{res} \approx 1/\sqrt{L(C_g + C_{total})}$$

$$R_{in} \approx L/R_{bias}(C_g \| C_{total})$$

$$V_{gs}/V_s \approx R\sqrt{(C_g \| C_{total})/L}$$ Passive

Half Circuits

1



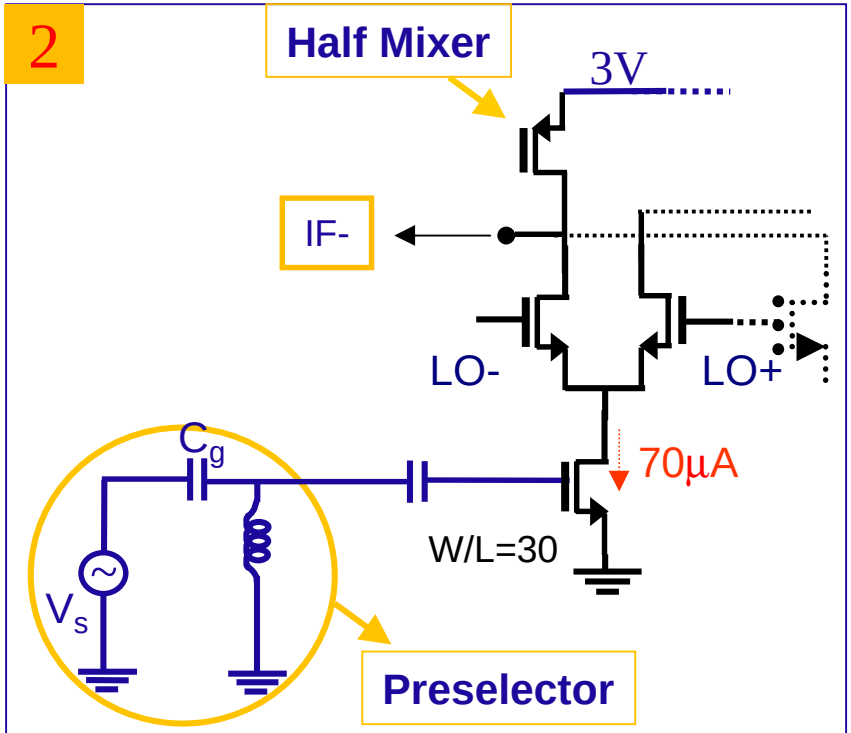
- LNA output impedance at ω_{res}:

  $\mathbf{R_{equ} = L / RC_{total}}$

Total gain:

$\mathbf{A_v = gm \cdot R_{equal} \cdot A_{preselector}}$

2



- High output impedance: Using active loads

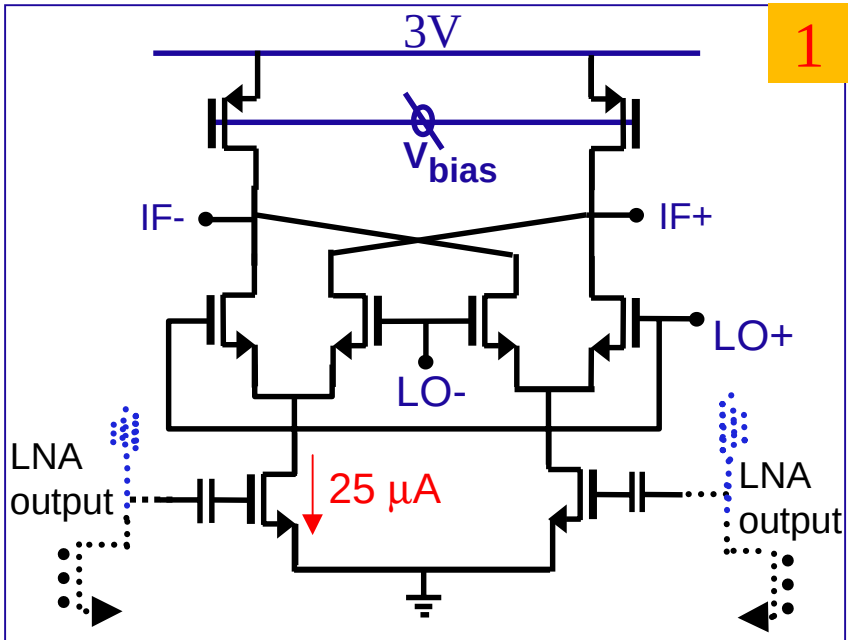
Total gain:

$\mathbf{A_v = gm \cdot R_{equal} \cdot A_{preselector}}$

Mixers

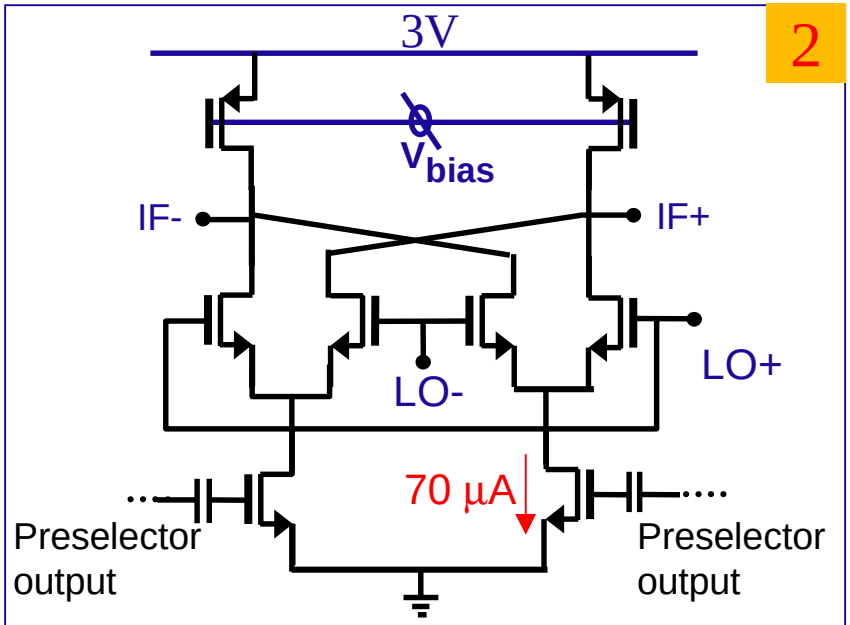
- Double-balanced Gilbert cell
- Direct conversion
- High output impedance
- Output bandwidth > 100 kHz

1



- Current consumption = 50 µA

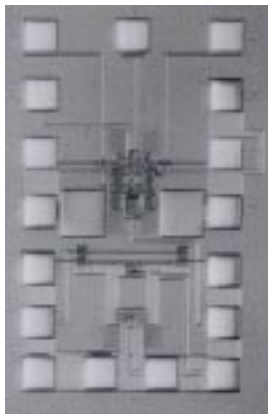
2

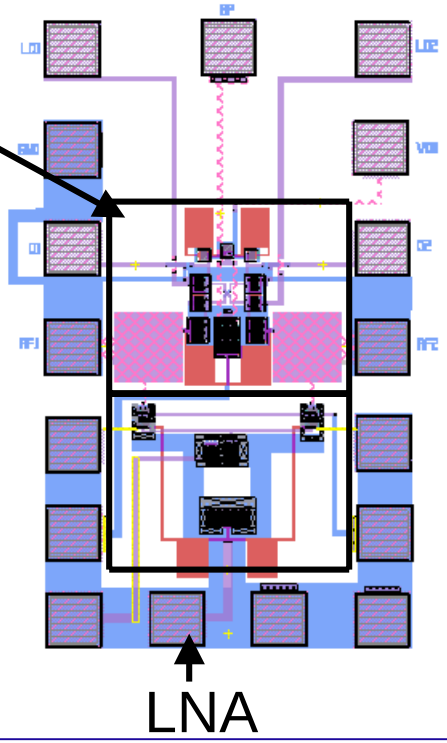


- Current consumption = 140 µA

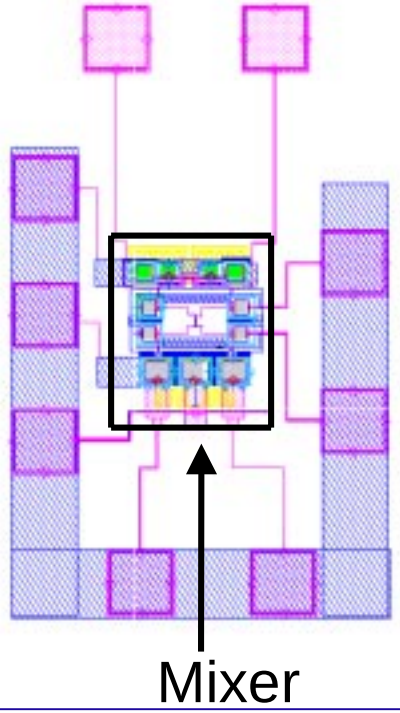
Layout and picture of the Front-end boards

- Multiple stage architecture, 0.8 μm technology

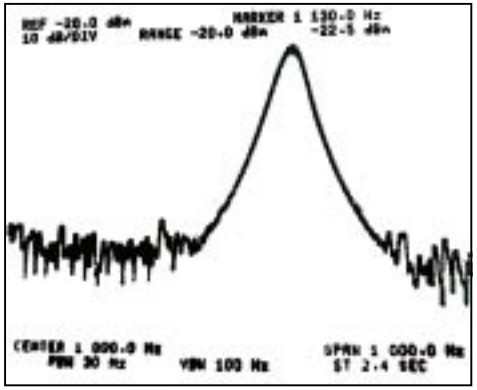
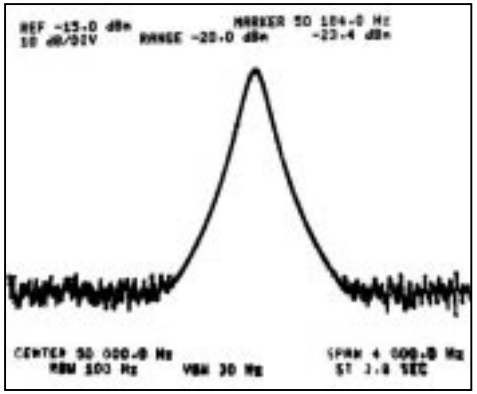
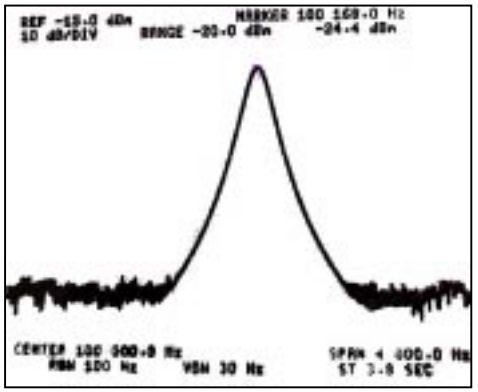
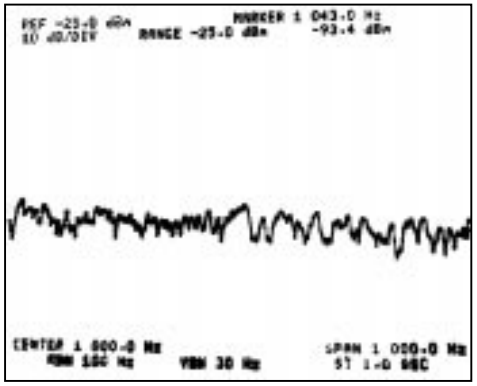
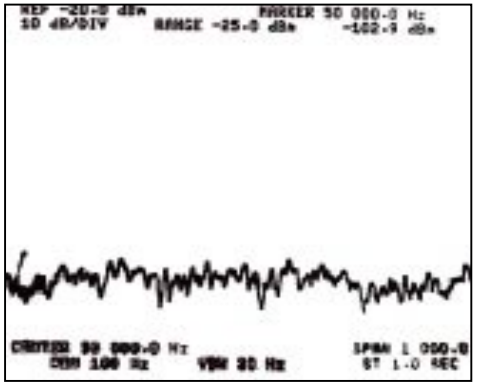




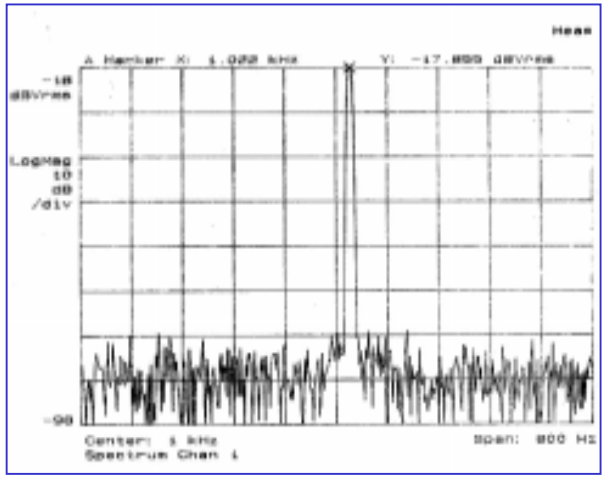
- Single stage architecture, 0.6 μm technology



Gain/ Noise Measurements
Single stage Architecture

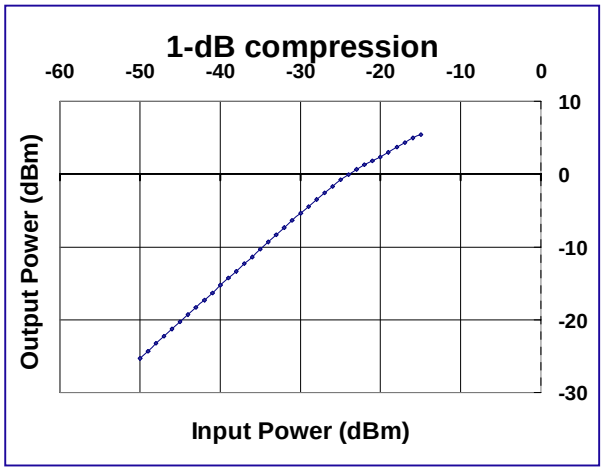
1 kHz	50 kHz	100 kHz
		
Gain = 30 dB	**Gain = 29.5 dB**	**Gain = 29 dB**
		
Noise = 27 dB	**Noise = 17.5 dB**	**Noise = 16 dB**

Gain/ Noise/ 1dB Measurements
Multi stage Front-end

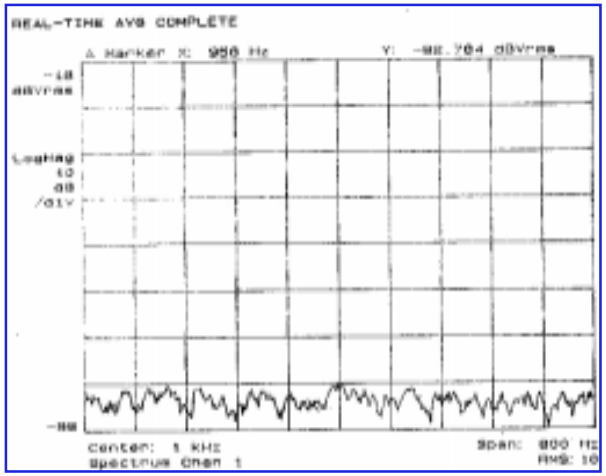


LNA input = -43dBvrms
Mixer output = -17.85dBvrms
Gain = 25 dB

1-dB compression
at -25dBm
(effective power)



This front-end:
At 1KHz: NF ≈ 28dB
At 25KHz: NF ≈ 19.5 dB



Comparing the results at 1khz and 25 kHz

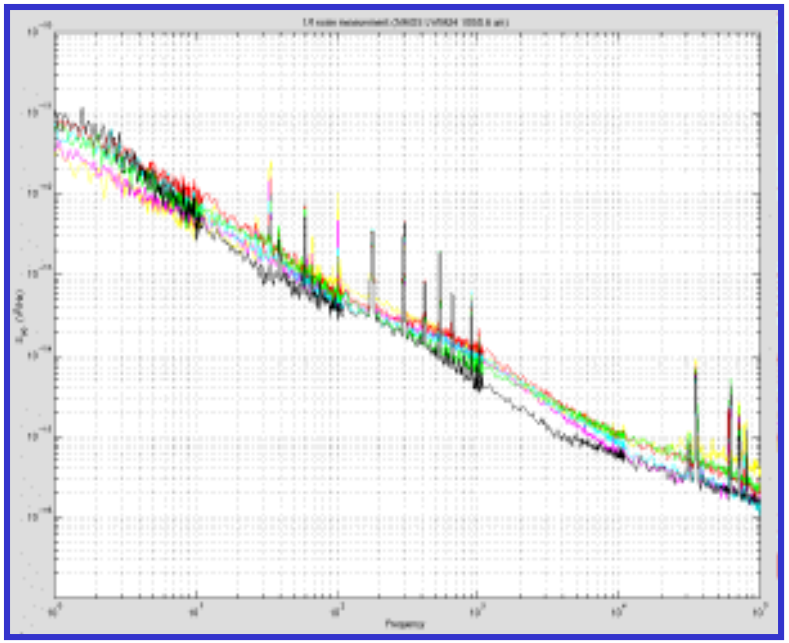
- Multi stage Architecture (0.8 μm)

	@1khz	@25khz
Gain	25 dB	24dB
Noise	26 dB	19.5dB
IP3	-15 dBm	-15 dBm
1dB	-25 dBm	-25 dBm

- Single stage Architecture (0.6 μm)

	@1khz	@25khz
Gain	30 dB	30dB
Noise	27 dB	21 dB
IP3	-13 dBm	-13 dBm
1dB	-23 dBm	-23 dBm

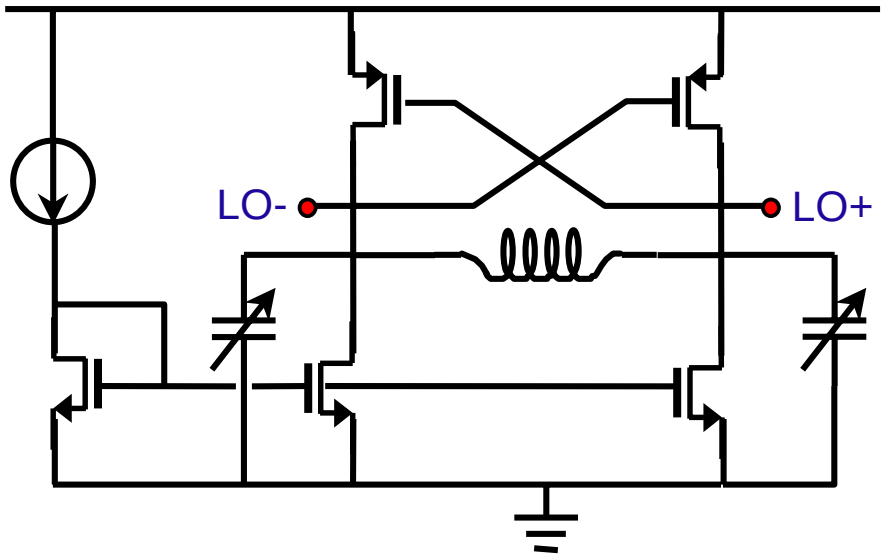
Final Results for Single Stage Front-end



1/f S_{VG} measurement
(NMOS 100/0.6 μm)

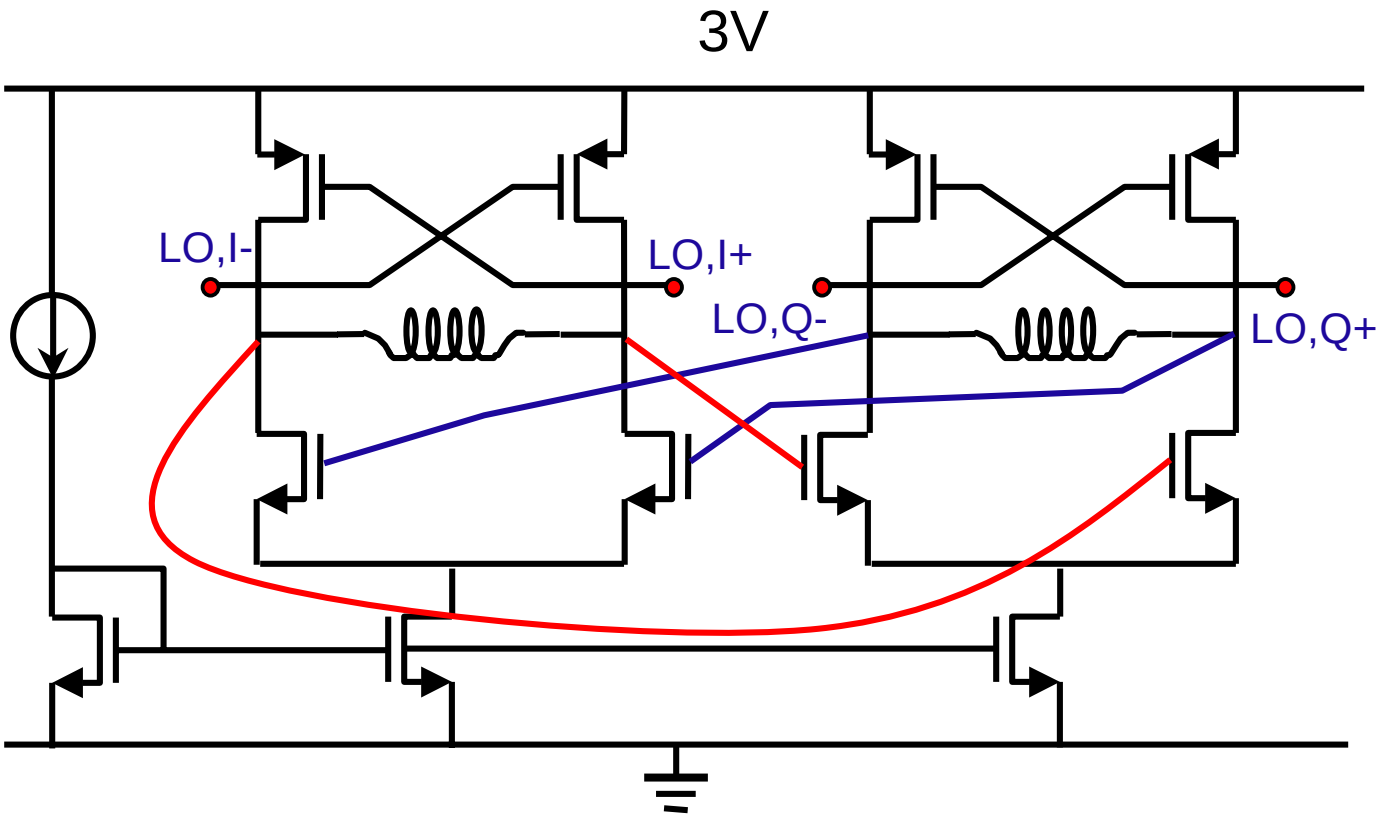
	@100kz
Gain	29 dB
Noise	16 dB
IP3	-13 dBm
1dB	-23 dBm

VCO Architecture



- HP CMOS 0.6 μm
- Cross-coupled PMOS transistors
  - isolated Nwell
  - less flicker noise
  - lower mobility
- Off-chip LTCC inductors
- MOSFET varactor tuning
- 3V, 150 μ A
- -100 dBc/Hz @ 100 kHz
- 10 % tuning range

Micropower CMOS Quadrature VCO

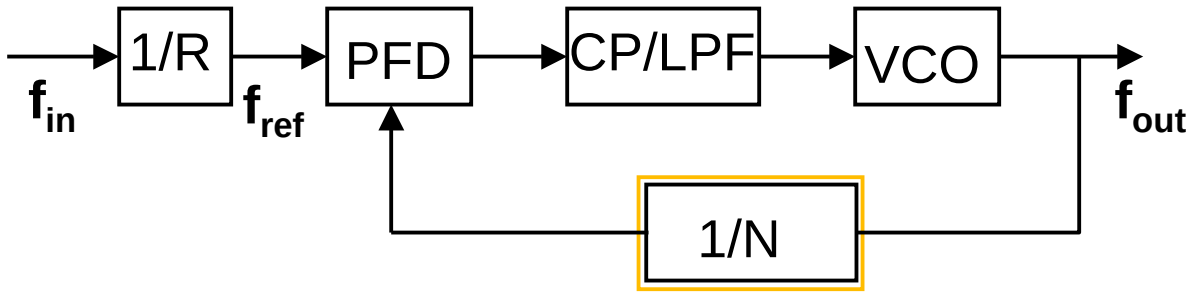


Frequency Synthesizer Design

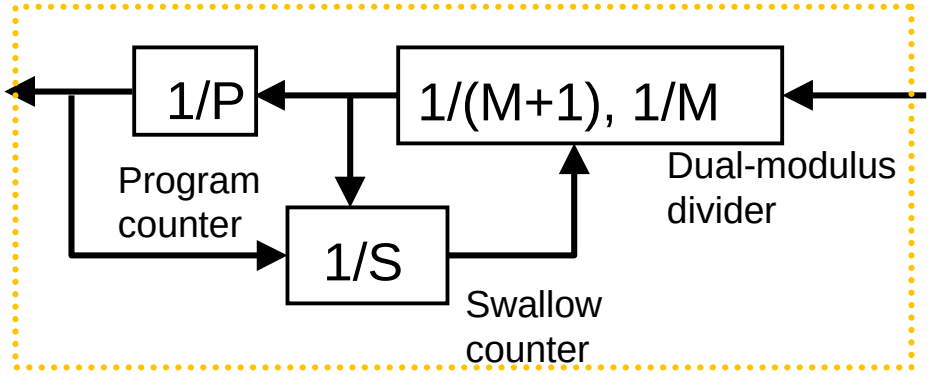
- Frequency synthesizer requirements:
  - switching time: less than 2 msec is adequate (depends on applications, usually latency tolerant)
  - frequency resolution: 250/500 kHz
  - low power operation: less than 1.5 mA drain current
- Frequency synthesizer techniques:
  - direct digital frequency synthesizer: fast switching, fine frequency resolution, but very high power (~1W, 12-bit, 100 MHz)
  - PLL: complex tradeoffs among frequency resolution, switching speed, and spurs; possible low power solution
- PLL architecture:
  - integer-N architecture (wide channel spacing and relaxed switching time requirements permit this low power PLL architecture)
- Design strategies:
  - high-Q LC-VCO: enables low power and low phase noise performance

Integer-N PLL

$f_{ref} = f_{in}/R$
$f_{out} = N.\ f_{ref}$
$N = (M+1)S+(P-S)M$
$= MP+S$
$f_{out} = (MP+S)f_{ref}$



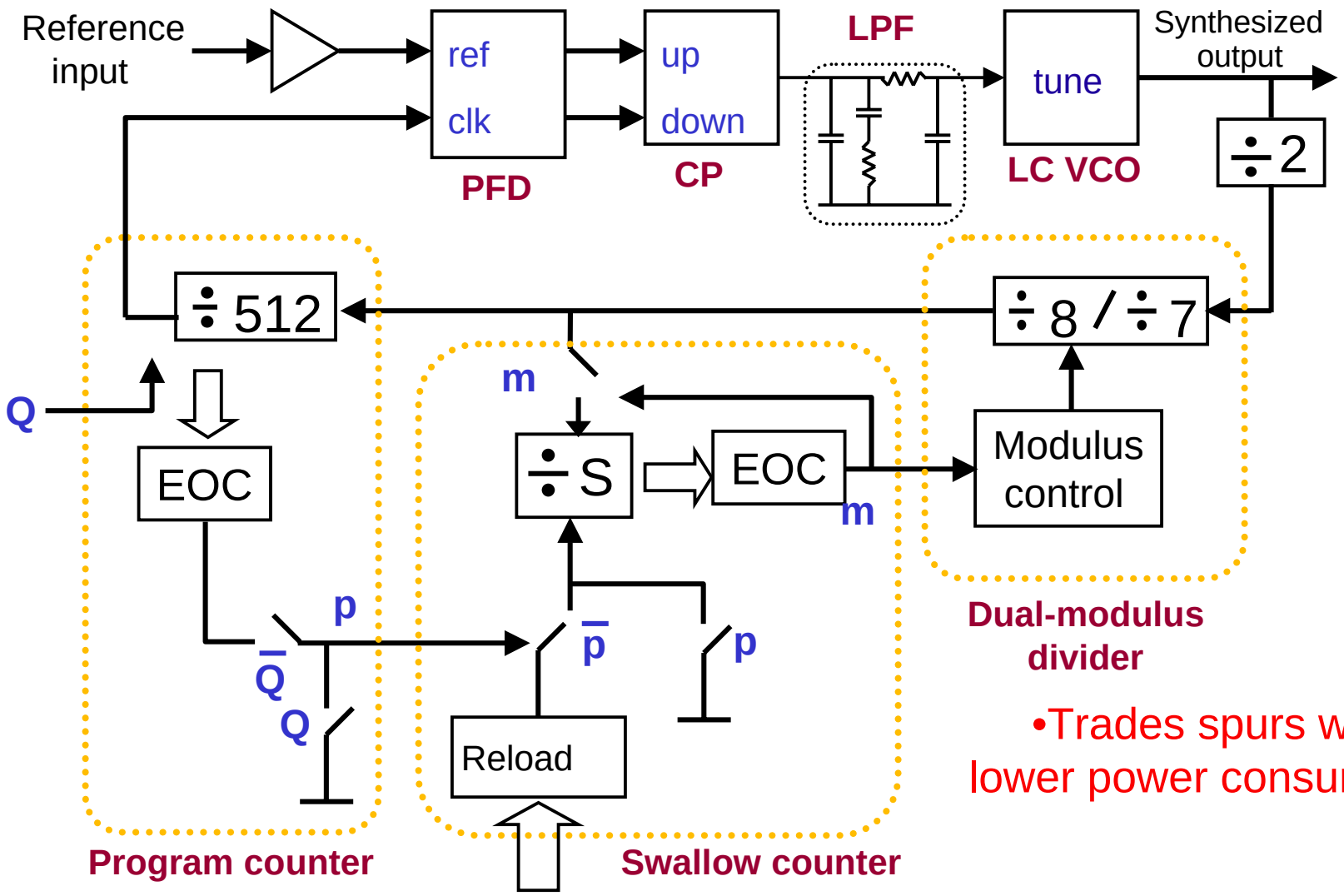
- To design lowpower:
- Wide channel spacing
- Relaxed switching time



f_{ref}=250 kHz, f_{out}=902~928 MHz ⇒ N=3609~3711 ⇒ M=7, P=512, S=25~127

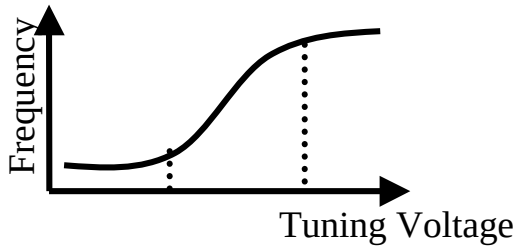
Dual-modulus divider (1/7,1/8) is the most power hungry component (operated at near 1GHz) in the PLL.

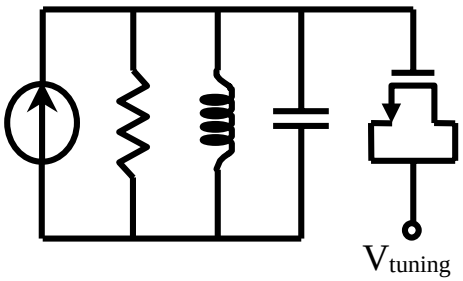
Modified Integer-N PLL Architecture



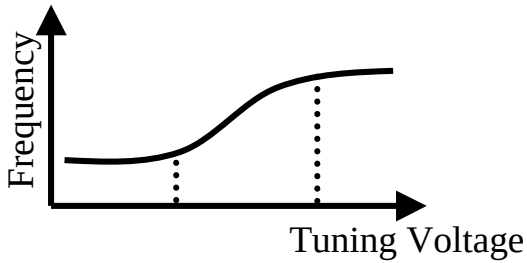
- Trades spurs with lower power consumption

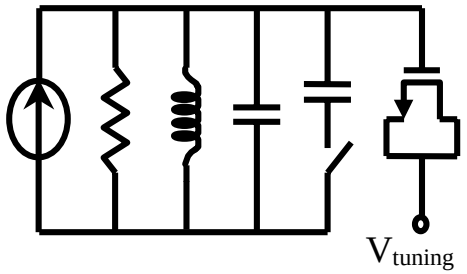
VCO Tuning





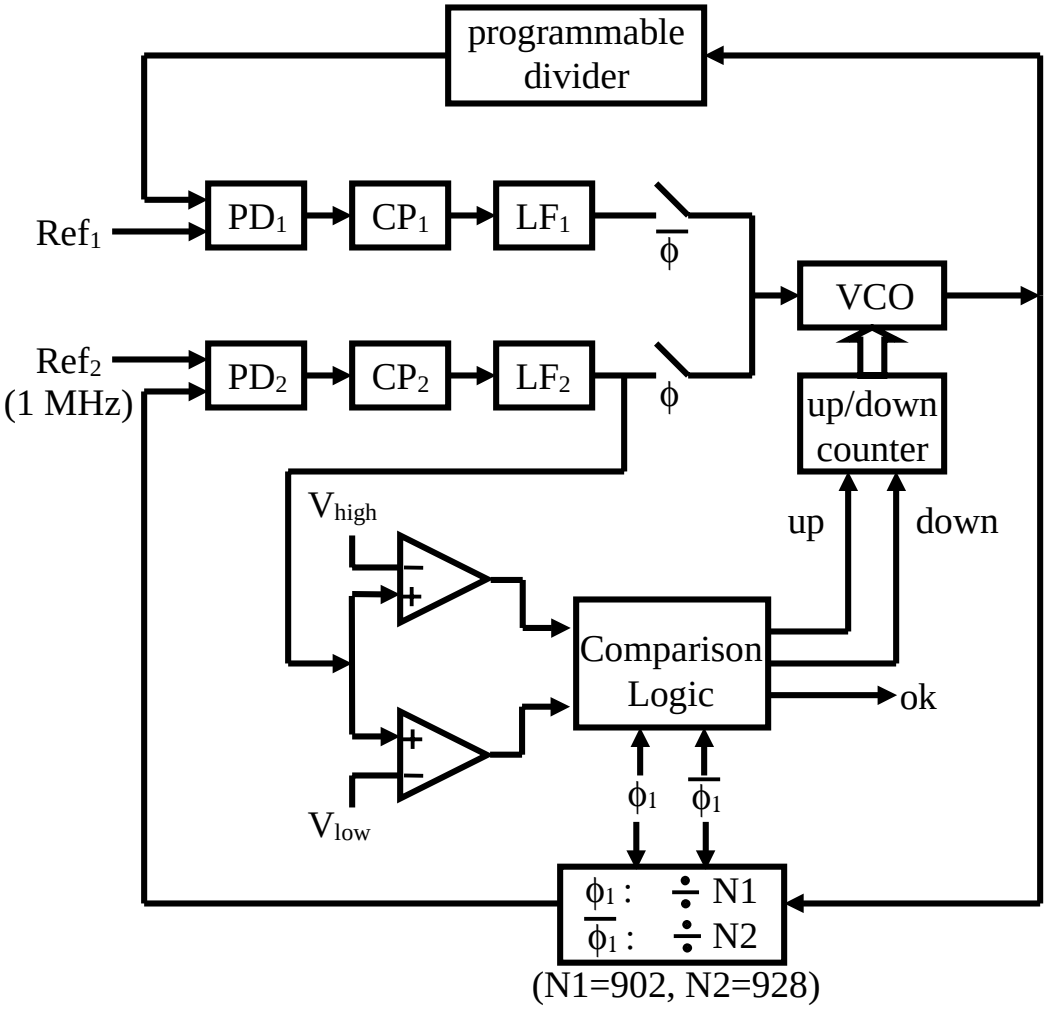
- CMOS varactor : 20-30% of tuning range to compensate for process and temperature variation
- sensitive to noise at VCO tuning node

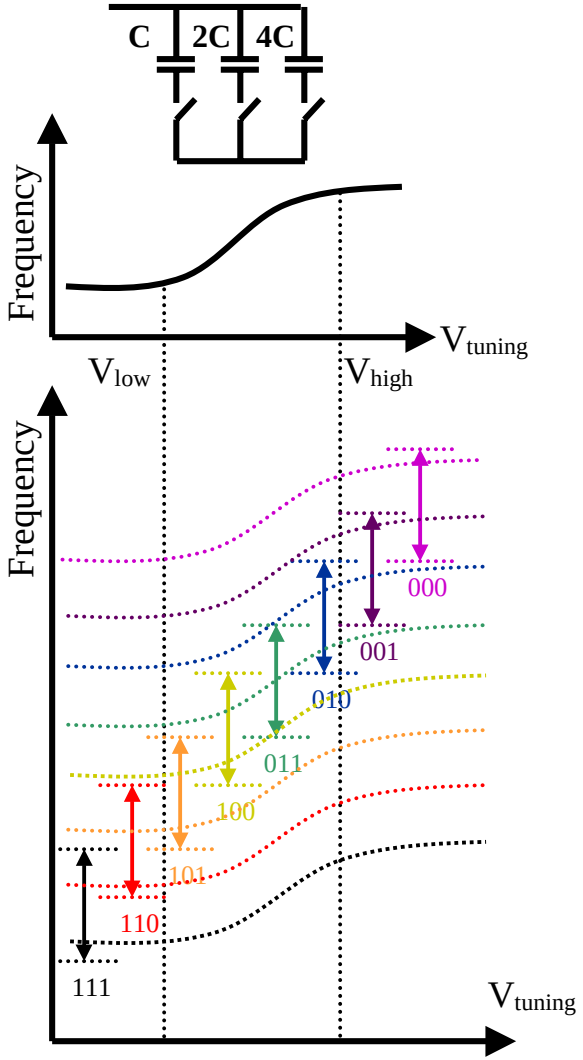




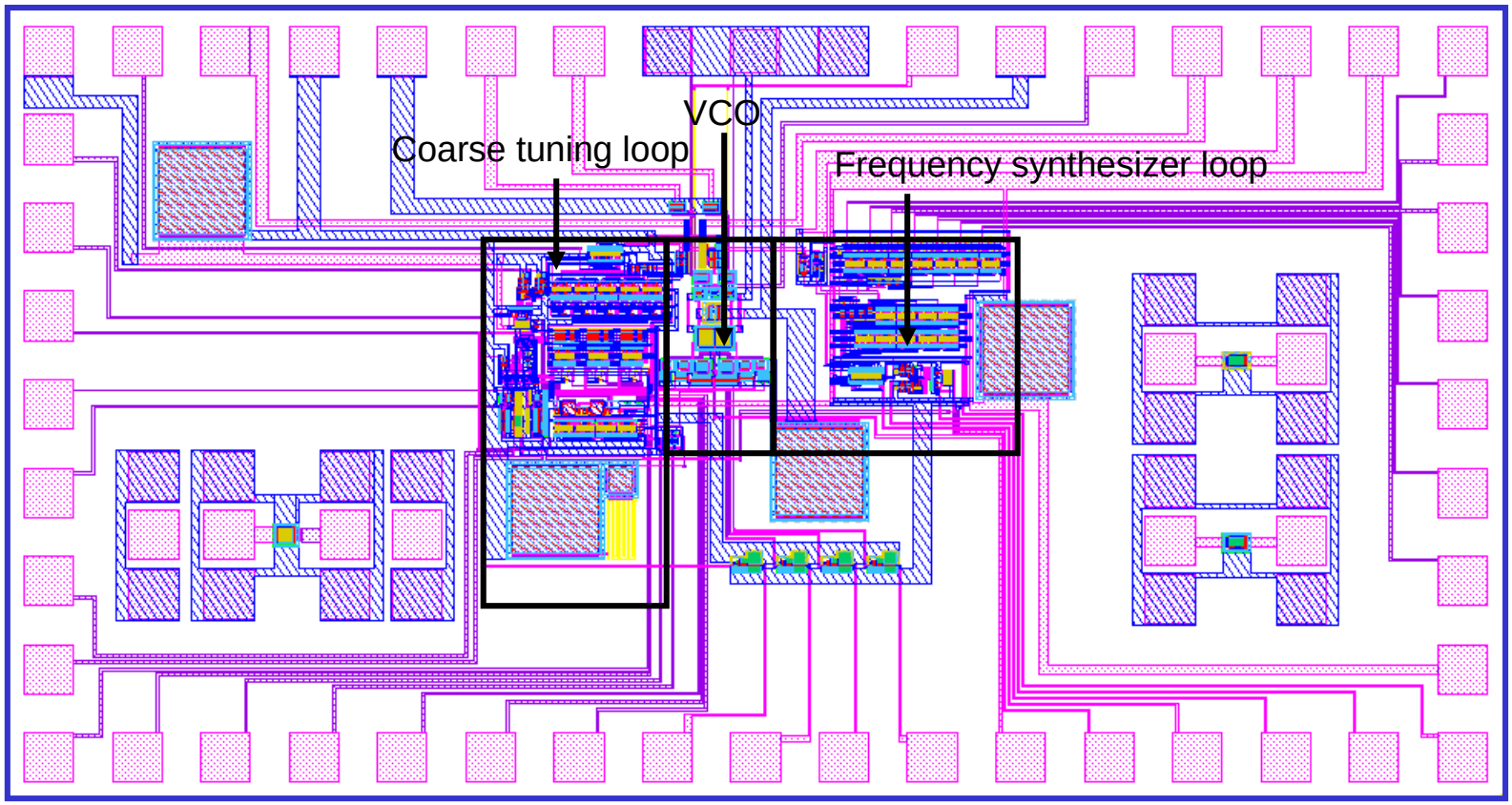
- Switched-capacitor provides coarse tuning
- CMOS varactor : fine tuning (much less tuning range is required in LC-VCO)
- less sensitive to noise

PLL with Coarse Tuning Loop



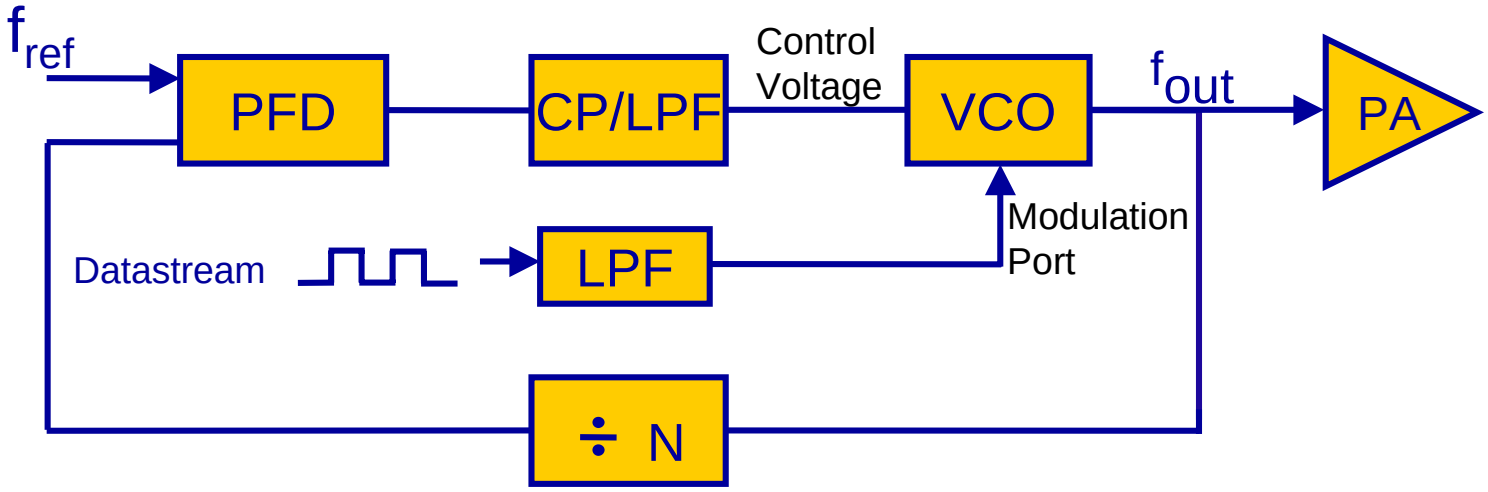


Layout



- HP 0.5um CMOS process
- Chip size: 2.6mm x 1.3mm

Transmitter Design

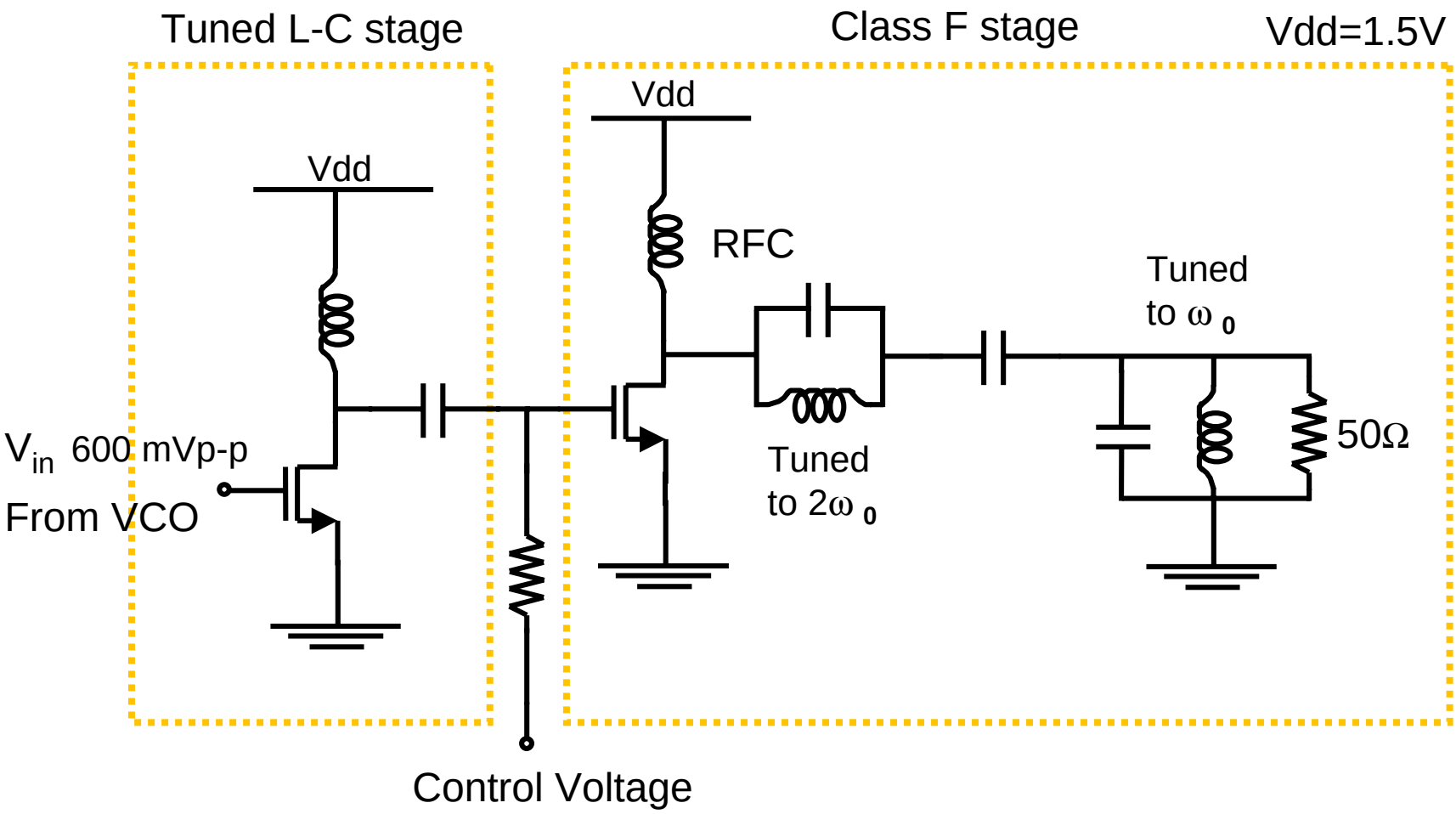


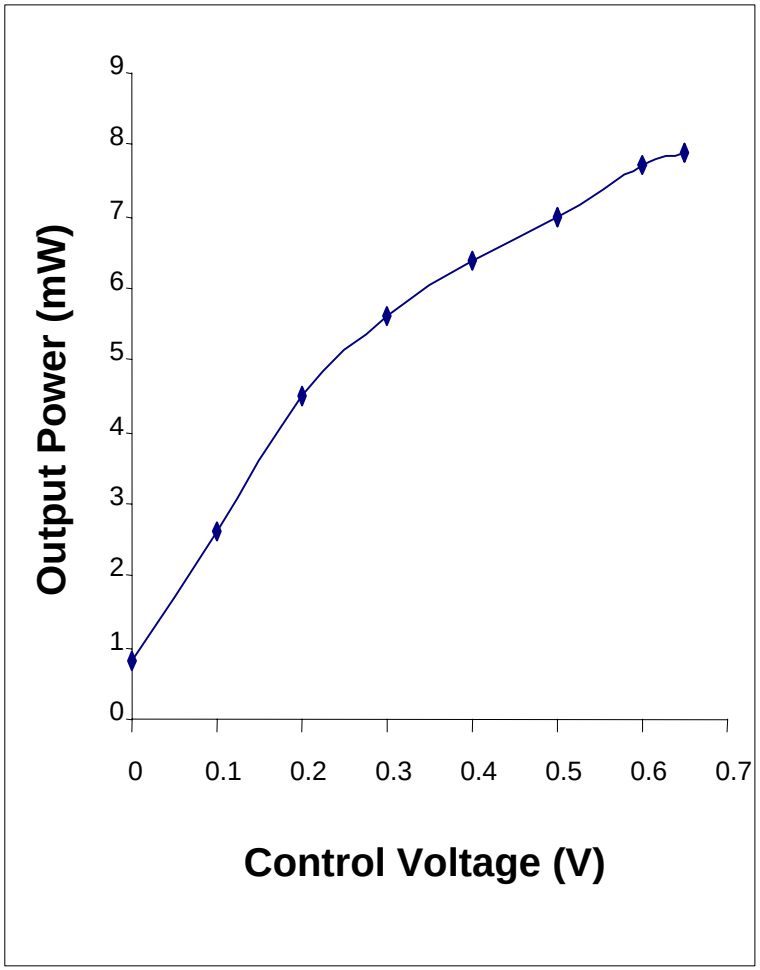
- Direct Modulation of VCO performed in Synthesizer Loop
- Loop bandwidth significantly less than frequency of modulation signal applied to VCO
- Mixerless design reduces power consumption
- Resistance to Injection Locking

Power Amplifier Design

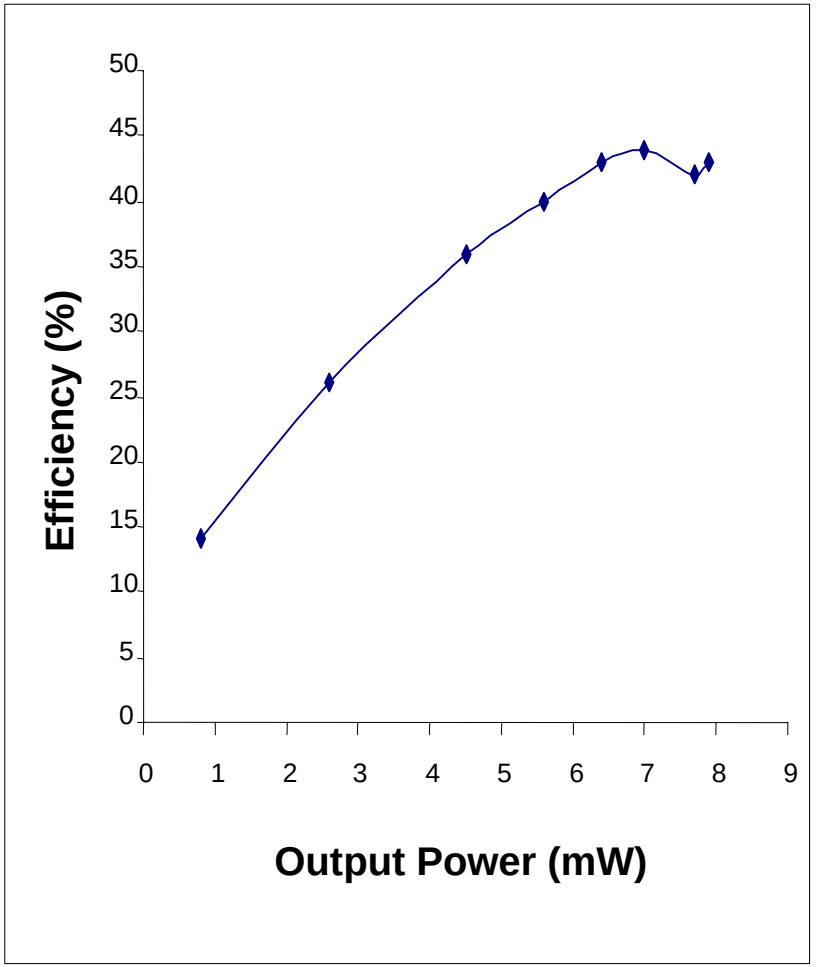
- Goal: To achieve low output power with high efficiency
- FSK system allows for use of non-linear power amplifier resulting in greater efficiency
- Variable output power desirable in order to deliver required signal strength at receiver, leading to overall system efficiency
- Efficiency is difficult to maintain over variable power range
- Power dissipation of predriver is increasingly important as desired output power decreases
- Variable PA with output powers ranging from 7mW to .5mW with efficiencies of 43% to 10% currently under development

PA Circuit


Tuned L-C stage
Class F stage
Vdd=1.5V
Vdd
Vdd
RFC
Tuned
to ω 0
V_{in} 600 mVp-p
From VCO
Tuned
to 2ω 0
50Ω
Control Voltage



Output Power vs. Control Voltage

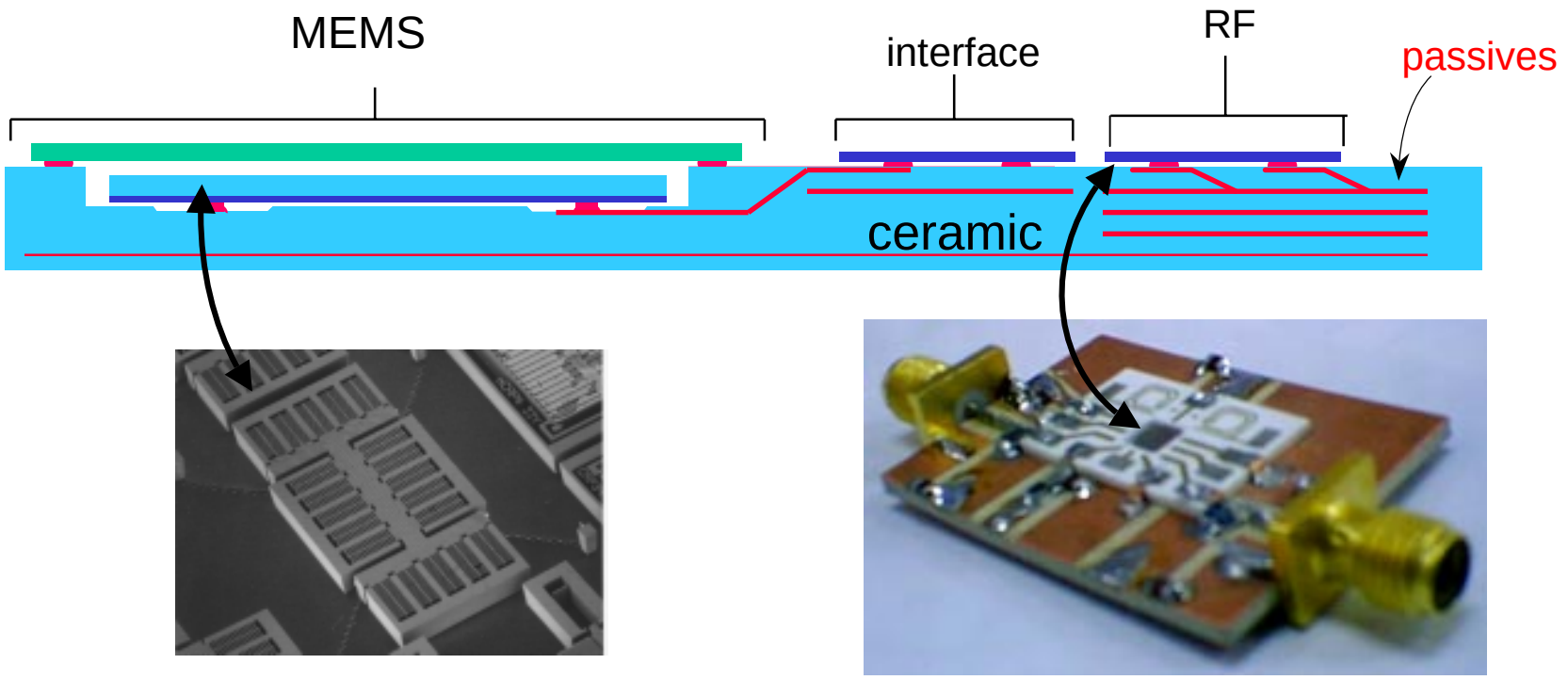


Efficiency vs. Output Power

WINS integration

- Low Temperature Co-fired Ceramic

L = 20nH Q ≈ 20 @ 1GHz



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Summary

- WINS project RF components trade off sensitivity for greatly reduced power consumption
- A front-end receiver with a total current consumption of 140 μA has been developed and tested in 0.6 μm CMOS technology
- The front-end includes a preselector which provides gain and filtering before the LNA
- The receiver has: Gain = 30dB, NF = 16dB, 1-dB compression = -23dBm

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- Scrantom Engineering, Inc. (SEI)
- Ms. M.Rofougaran, Dr. D. Pelhke

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